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An investigation was undertaken to design and fabricate low noise, high speed InP-based HEMTs. The investigation consisted of several components: the development of quantum corrected hydrodynamics simulation codes; application of these codes to aid in design and optimization of HEMTs for low noise, high speed operation; and fabrication and testing of the resulting designs. Through the research effort, HEMTs of previously unobtained performance levels were designed and fabricated. These results showed that the use of simulation can play a significant and important role in extracting performance from proposed device structures, and should be used as an integral part of the design process.

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DESIGN AND DEVELOPMENT OF LOW NOISE, HIGH SPEED, HIGH ELECTRON MOBILITY TRANSISTORS (HEMTS)

FINAL REPORT SRA R94-9335-F

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I. INTRODUCTION

Recent advances in crystal growth and processing techniques have made possible the fabrication of devices with sharp, well-defined interfaces. One such device is the quantum well HEMT shown in Fig. 1. In such structures, a 2-DEG is created in an undoped channel through seeding via a planar doped layer in an adjacent wide gap material. This same wide gap material layer also acts as a gate isolation layer. Quantum well HEMT structures have been fabricated from GaAs/AlGaAs, GaAs/GaInP, AlGaAs/InGaAs and InGaAs/InAlAs. There has been considerable experimental research on InP-based HEMTs. In particular, $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ lattice matched and pseudomorphic structures on InP substrates have received much attention [1] - [13]. This system is favored over the others because it has demonstrated superior noise and gain performance at high frequencies. The high conduction band discontinuity and lower effective mass leads to better confinement of higher density 2-DEGs and the improved high frequency performance. Noise figures as low as 0.8 dB have been reported [1] for a 0.2 μm gate structure.

This investigation is directed at continued research in the design and development of InP based PHEMTs for high speed, low noise application with 0.1 μm gate widths. The research effort is composed of two parts; analytical analysis of wafer structures and simulation of processed devices, and fabrication and experimental evaluation of fabricated devices. The analysis and simulations were performed by Scientific Research Associates, Inc. using software, developed as part of this effort, based on the quantum corrected hydrodynamic equations. The fabrication and experimental aspect of the investigation was handled under subcontract to the Martin Marietta Corporation Electronics Laboratories. The interaction involved a continual exchange of

information and progress throughout the development procedure. For example, wafer structures were proposed, then simulations performed to evaluate the proposed structures. Based on the simulations, specific wafer structures were processed into HEMTs and measured. Full device simulations were then performed of these structures to validate the HEMT simulation procedure. Then, based on the simulation and experimental results, new structures were proposed and evaluated using the simulation procedures. These results were used to screen the proposed improved structures prior to device fabrication. The simulated structures with highest predicted performance were then processed and measured experimentally. This interactive procedure resulted in achieving fabrication of devices with extremely high performance figures rendering such an interaction as highly successful.

While the interaction between analysis, fabrication and experimental measurement was continuous over the research effort, we shall present the results of each aspect separately with an indication of the interplay sited appropriately. We shall first present an analysis section dealing with the development of our simulation procedures, development of workstation interfaces for our wafer simulations and applications of full two-dimensional simulations to study various factors which influence device performance. Next we will present the initial phase of the experimental effort and discuss initially proposed wafer structures, what simulated results indicated about these structures, and the measured performance of devices fabricated from these initial wafers. We will then address proposed modifications to the wafer structure and what simulation revealed about these modifications. Finally, we shall present the results for an optimized device structure.

II. QUANTUM HYDRODYNAMIC MODEL FOR HEMT SIMULATION

There are numerous factors which may influence the behavior of HEMTs with structures as shown in Fig. 1. These include (1) the doping of the cap layer, (2) the depth of the gate recess, (3) the planar layer sheet charge density, (4) the thickness of the spacer layer and (5) the depth of the channel. As part of this study we examine the influence of these parameters on a generic device's performance through simulations based on a set of quantum corrected hydrodynamics equations. The need to include quantum mechanical corrections in the simulation is dictated by the presence of sharp, abrupt interfaces between the various material layers of the device. These interfaces give rise to quantum mechanical effects which are paramount in determining the distribution of charge within the device, and particularly in the creation of the 2-DEG in the channel.

There have been a variety of developments of quantum corrected hydrodynamic equations which have appeared in the literature (Refs. [14] - [16]). The form we are presently employing in our simulations is given, in one dimension, as:

1) $$\frac{\partial n}{\partial t} = -\frac{\partial nu}{\partial x}$$

2) $$\frac{\partial u}{\partial t} = -u\frac{\partial u}{\partial x} - \frac{k_o}{mn}\frac{\partial Tn}{\partial x} + \frac{q}{m}\frac{\partial}{\partial x}\left(\psi + \psi_c + \frac{Q}{\alpha}\right) - \frac{u}{\tau_m}$$

3) $$\frac{\partial e}{\partial t} = -u\frac{\partial e}{\partial x} - (k_o T - Q_e)\frac{\partial u}{\partial x} + \frac{1}{n}\frac{\partial}{\partial x}\left(\kappa\frac{\partial T}{\partial x}\right) - \frac{(T - T_o)}{\tau_e} + \frac{u^2}{\tau_m}$$

and

4) $$\frac{\partial}{\partial x}\left(\varepsilon\frac{\partial \psi}{\partial x}\right)=q(n-N_D).$$

The Bohm potential [17] is defined as

5) $$Q=\frac{\hbar^2}{2m}\frac{1}{\sqrt{n}}\frac{\partial^2\sqrt{n}}{\partial x^2}$$

The internal energy, e, is given as

6) $$e=\frac{3}{2}k_0T-\frac{Q_e}{2}.$$

where Q_e is the Wigner potential [18] defined as

7) $$Q_e=\frac{\hbar^2}{12m}\frac{\partial}{\partial x}\left(\frac{1}{n}\frac{\partial n}{\partial x}\right)$$

In Eqs. (1-6), n is the electron density, u is the electron velocity, T, is the temperature of the electron gas, m is the effective electron mass, e is the "quantum corrected" internal energy of the electron gas, N_D is the donor doping level, ψ is the self-consistent electrostatic potential, and τ_m and

τ_e are momentum and energy relaxation times. The potential ψ_c is introduced to account for variation in the conduction band and is related to the electron affinity of the local material,

$$8) \qquad \psi_c = -\frac{\chi}{q}.$$

The factor, α, appearing in Eq. (2) is treated as an adjustable parameter. A value of $\alpha = 3.0$ has been found to yield results which are in excellent agreement with solutions to the Liouville equation for single barrier structures [19]. We have previously used a variant of the momentum equation, Eq. (2), in which the term representing the gradient of the conduction band energy level was eliminated in favor of one involving the gradient of the Fermi level [20]. This was originally done to eliminate taking derivatives across the discontinuities in the conduction band. However, our experience has shown that while ψ_c and Q may exhibit discontinuous behavior, the effective conduction band energy, $E_t = -q(\psi + \psi_c + Q/\alpha)$, is continuous, even across abrupt interfaces. We have therefore reverted to the form of Eq. (2) since it yields the same results while reducing the complexity of our solution algorithm.

The relaxation times in the present simulations have been related to the uniform field velocity field relationships for the material considered. Under the assumption of a uniform field, the momentum equation, Eq. (2) reduces to:

$$9) \qquad u = \frac{\tau_m e}{m}\frac{\partial}{\partial x}\left(\psi + \psi_c + \frac{Q}{\alpha}\right) \equiv -\mu F$$

where μ is a mobility and F the effective electric field resulting from the gradient of the conduction band energy including the contribution from the quantum potential. From Eq. (9) we arrive at the relationship:

$$10) \qquad \tau_m = \frac{m\mu}{e}.$$

To account for the energy dependence of the relaxation time we introduce a field dependence:

$$11) \qquad \mu(F) = \frac{\mu_0}{\left\{1+\left(\frac{\mu_0(|F|-|F_0|)}{V_{sat}}\right)^{\alpha}\right\}^{1/\alpha}}$$

where μ_0 is the low field mobility, V_{sat} is the saturated drift velocity which would exist under uniform field conditions, F_0 is the zero bias, equilibrium field and α is constant between 1 and 2. The magnitude of the field, $|F|$, is reduced by the magnitude of the equilibrium field, $|F_0|$, since F_0 does not contribute to the carrier energy. The energy relaxation time is then taken as 0.5 times τ_m. We note that the use of the above approximations does not imply that the velocity is in equilibrium with the local field, nor does it imply that the maximum velocity obtainable is equal to V_{sat}. Under nonuniform field conditions the velocity may exceed V_{sat} locally.

It is recognized that a more complex relationship than Eq. (11) can be introduced in which a negative differential mobility is specified. However, we again note that such relationships apply only to uniform field conditions at local equilibrium. Furthermore, we must not confuse velocity

overshoot effects resulting from nonuniform, nonequilibrium spatial transport to negative differential mobility.

We must also have a sound idea of the length scales over which quantum effects are important. This is necessary in determining a suitable grid structure in a simulation, as well as to provide insight with regard to the physics of a given problem. We recognize from both Eqs. (2 & 5) that if the quantum potential is to have a first order effect on momentum transport or density at an interface, then it must be of the same order of the potential difference in the conduction band, $\Delta\psi_c$. From Eq. (5) we see that this requires that $\hbar^2/\left(2mx^2\Delta\psi_c\right)$ must be of order one. Using typical values for m and $\Delta\psi_c$, a length scale of the order of 10 Å emerges. Thus, if quantum effects are to be important, interfaces must be very sharp. Grading interfaces over 100 Å or more will significantly reduce the transport due to quantum effects. This analysis also tells us that if we are to accurately resolve quantum effects in our simulations, we must employ computational grids with spacings of the order of one angstrom at abrupt interfaces. In the simulations presented here we have used grid spacings as small as 0.5 Å in our 1-D computations and 4.0 Å in the 2-D results, to ensure accurate resolution.

III. THE COMPUTATIONAL PROCEDURE

Equations (1) - (7) form a coupled system of nonlinear partial differential equations which must be solved. In order to solve these equations numerically the equations must be linearized and then the resultant system must be discretized in space and time. We note that as written the highest

order derivative which appears is of second order. Thus, a three point spatial differencing approximations can be applied and, in one dimension, the resulting matrix system of linear equation would be block tridiagonal in structure. There exist straightforward procedures for solving block tridiagonal systems and, in this system, boundary conditions are easily applied. We note also that the Bohm and Wigner potential could be substituted directly into the remaining equations with a reduction in the number of equations to be solved from seven to five. However, the order of the highest derivative now is raised to third. The higher order derivative will increase the bandwidth of the matrix system to pentadiagonal if a centered difference approximation is used and spurious boundary conditions will be required for the electron density. While these boundary conditions can be developed from specification of Q and Q_c on the boundaries, the added bandwidth can become cumbersome. Thus, we chose to retain the equations for Q and Q_c and solve the coupled tridiagonal system of seven equations.

To solve the system of Eqs. (1)-(7) in one dimension we apply a linearized block implicit (LBI) procedure. We have successfully used this procedure in single and multidimensional simulations using the drift and diffusion equations and moments of the Boltzmann transport equation. The system of equations (1)-(7) may be expressed as

$$12) \qquad \frac{\partial H(\phi)}{\partial t} = D(\phi) + S(\phi)$$

where

13) $$\phi = \left[n, u, T, \psi, Q, Q_e, \psi_f\right]^T$$

and $H(\phi)$, $D(\phi)$, and $S(\phi)$ represent functions of the dependent variables. $D(\phi)$ represents the spatial operators and $S(\phi)$ source terms. The equations are linearized, for example, as

14) $$\begin{aligned} G(\phi)^{n+1} &= G(\phi)^n + \Delta t \frac{\partial G(\phi)}{\partial \phi}\left|\frac{\partial \phi}{\partial t}\right|^{n+1} + O\left(\Delta t^2\right) \\ &\approx G(\phi)^n + \left.\frac{\partial G(\phi)}{\partial \phi}\right|^n \Delta \phi^{n+1} + O\left(\Delta t^2\right) \end{aligned}$$

where the superscript indicates a time level,

15) $$t^{n+1} = t^n + \Delta t.$$

Performing the linearizations and collecting terms results in the equation

16) $$(A + \Delta t L)\Delta \phi^{n+1} = \Delta t\left[D\left(\phi^n\right) + S\left(\phi^n\right)\right]$$

where

17) $$A \equiv \left(\frac{\partial H}{\partial \phi} - \Delta t \frac{\partial S}{\partial \phi}\right)^n$$

and

18) $$L \equiv -\left.\frac{\partial D}{\partial \phi}\right|^{n}.$$

Equation (16) represents a 7x7 block coupled system of linear partial differential equations. Introducing a computational mesh of N grid points and employing three point centered difference operators to approximate the operator L, equation (16) may be expressed as

19) $$M\Delta\phi = B$$

where M is an NxN block tridiagonal matrix with 7x7 block size. The narrow banded block structure allows for efficient solution of Eq. (19) using direct methods.

When multidimensional problems are considered the narrow band structure of the M matrix is lost. If a two-dimensional problem is considered on an NxN mesh then the M matrix will be of rank N^2 and the bandwidth will be N. However, the matrix may be split using ADI techniques [21] to reduce the two-dimensional matrix to a series of one-dimensional matrices. Letting the L operator be expressed as the sum of the x and y direction operators,

20) $$L = L_x + L_y$$

equation (16) can be split as

21a) $$(A+\Delta tL_x)\Delta\phi^* = \Delta t\left[D(\phi)+S(\phi)\right]^n$$

21b) $$\left(A+\Delta tL_y\right)\Delta\phi^{**} = A\Delta\phi^*$$

and

$$\Delta\phi^{**} = \Delta\phi^{n+1} + O\left(\Delta t^2\right).$$

Each of equations (21) is block tridiagonal and of rank N. Each is repeated N times in the x and y directions, respectively. The result is a significant reduction in computation at the expense of introduction of some additional error due to the splitting. As the solution converges, the splitting error goes to zero and the solution to Eq. (16) is recovered.

We note however, that direct application of Eq. (21) to the multidimensional system is not possible. The lack of a time derivative or a source term involving ψ is Poisson's equation causes the A matrix, given by Eq. (17), to be singular which makes application impossible. This can be corrected by either adding a pseudo time derivative to Poisson's equation, or be decoupling Poisson's equation from the system. Other modification to the algorithm are also possible. We generally decouple Poisson's equation in multidimensional problems since this has to be found to be stable and reduce the block size of the coupled system, improving efficiency of the solution algorithm. Poisson's equation is then solved sequentially, using any appropriate method for elliptic equations, at each time iteration.

IV. ONE-DIMENSIONAL WORKSTATION INTERFACE

One of the important aspects of the design and development of a new high performance device is the ability to rapidly and accurately screen preliminary structures for characteristics which are favorable to the desired performance parameters. Under the present effort, which addresses high speed, low noise HEMTs, an important step in the design is to be able to evaluate the potential of proposed wafer structures before their growth and prior to fabrication of such wafers into the device. Here one-dimensional analysis plays a significant role. For example, Fig. 2 shows the general wafer structure for the quantum well HEMTs considered in this investigation. As eluded to in our early comments, many factors influence the performance potential of such structures when processed to HEMTs. Many of these concern the creation of the 2-DEG in the device channel and can be evaluated within the framework of one-dimensional analysis. These factors include cap layer doping, planar layer doping density, spacer layer thickness, channel depth and depth of the gate recess. We shall discuss the results of investigating these factors using one-dimensional simulation and show their correlation with two-dimensional simulation results subsequently. We shall first discuss the workstation-based one-dimensional simulation procedure and interface developed as part of this overall effort.

In order to rapidly access the potential of a proposed wafer structure rapidly using one-dimensional simulation, it is necessary to be able to setup the structure quickly on a computer and then easily vary the structure. To accomplish this we have developed a windows-based workstation interface which is applicable to a variety of one-dimensional problems which can be modeled using the quantum corrected hydrodynamics equations. The control window of the

interface is shown in Fig. 3. The user can simply move the cursor across the screen and select the desired option. To begin, the user would select the "Define Device" option. By clicking on this button a new window is open, as shown in Fig. 4, which allows the user to define the doping, barrier structure and generate a computational grid. Choosing the "Define Doping" option opens the two windows shown in Fig. 5. The doping and barrier structure is shown graphically in the upper window. Both doping and barriers can be input using the graphic window. A point-and-click procedure using the mouse and cursor are used in this procedure. Alternatively, digital input can be specified using the lower window. The user would then return to the control window (Fig. 3) and proceed to the next highlighted buttons below "Define Device" in sequence. The case is then executed and when completed, the user may display results. As an example, we have displayed a graph of electron density in Fig. 6. This is for a wafer structure typical of that shown in Fig. 2. This density plot can be printed directly on a laser printer to yield a report quality figure, as shown in Fig. 7.

Having performed a simulation of a given structure, the user can then easily modify the structure by altering the channel thickness (the barrier structure), the cap layer doping, etc., and repeating the simulation. In this way the user can rapidly access the characteristics of a given device or wafer structure. We have found this software extremely useful during the course of the present investigation. Thus, not only was the software developed under the current effort, it played an integral part in the design and evaluation phases of the research.

V. DESIGN AND FABRICATION OF InP-BASED HEMTS

V.1. PRELIMINARY WAFER STRUCTURES

The design and fabrication of InP-based HEMTs was performed initially along parallel paths by Scientific Research Associates, Inc. and the Martin Marietta Electronics Laboratory*. During the initial portion of the research effort SRA developed and tested the one- and two-dimensional simulation tools while Martin Marietta proposed and grew four initial wafer structures. The four wafer structures were referred to as No. 3-1599, 3-1603, 3-1605 and 3-1800. All structures consisted of a 100 Å InGaAs cap layer doped to $1x10^{18}/cm^3$, a 200 Å undoped InAlAs gate isolation layer, and Si planar doped layer with a doping sheet density of $5x10^{12}/cm^3$. The structures varied under the PD layer. Structures 3-1599, 3-1603 and 3-1605 had a 45 Å InAlAs spacer layer following the PD layer, while the 3-1800 had a 42 Å spacer layer. Device 3-1599 then had a 130 Å $In_{0.75}Ga_{.25}As$ channel on 0.25 μm InAlAs. Device 3-1603 had a 275 Å $In_{0.65}Ga_{.35}As$ channel on InAlAs. Device 3-1605 had a 175 Å $In_{0.70}Ga_{0.3}As$ channel on InAlAs. Finally, device 3-1800 had a channel consisting of 400 Å $In_{.6}Ga_{.4}As$ followed by 400 Å of lattice matched InGaAs on InAlAs. The channel depth and mole fraction of In in the channel were varied to allow stable structures. The wafers are all of the general structure previously shown in Fig. 2. All structures were grown on an InP substrate.

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* Martin Marietta purchased the Electronic Laboratory from GE during the term of the contract.

V.2 SIMULATION OF WAFER STRUCTURES AND EVALUATION

Prior to processing these wafers to make the 0.1 μm gate HEMTs, SRA performed one-dimensional simulations of the wafer structures to examine the expected charge distribution in the 2-DEG. The PD layer was modeled as a 10 Å wide layer doped to $5x10^{19}/cm^3$ for a planar layer density of $5x10^{12}/cm^2$. The predicted distribution of charge of the four wafers, as obtained from the workstation software, is shown in Figs. 8a and 8b. The linear scale of Fig. 8a shows the peak density is greatest for structure 3-1599, followed by 3-1605. The lowest peak was for structure 3-1800. In Fig. 8b, the use of a log scale allows examination of the distribution lower density charge levels across the channel. Here the confinement by the heterojunction at the bottom of the channel is clearly evident. The distribution for structure 3-1800 also reflects the change in the band structure in the center of the channel where the mole fraction of In is reduced from 0.6 to 0.53. We also note that these figures were produced directly with the options of the workstation software. The charge sheet density for these structures is given in Table I. These numbers represent

TABLE I

Wafer No.	**Charge Sheet Density $1/cm^{-2}$**
3-1599	$4.20x10^{12}$
3-1603	$4.02x10^{12}$
3-1605	$4.11x10^{12}$
3-1800	$3.98x10^{12}$

the sheet density of mobile electrons in the channel. Most of the electrons from the PD layer accumulate in the channel at the spacer layer-channel interface, as indicated in Fig. 8. However, some of the electrons migrate to the interface between the cap layer and the gate isolation layer, as is also observable in Fig. 8.

Before processing of the wafers we examined the predicted results with consideration of high frequency and noise performance. From the consideration of high frequency, a high transconductance is desirable. This requires high conductance in the channel, thus a high charge sheet density is a prerequisite. The most favorable wafer in this regard was wafer number 3-1599, followed by wafer 3-1605. Wafers 3-1603 and 3-1800 were very similar in this regard, but below the levels of the other two.

From consideration of the noise level, we recognized that these HEMT structures are unique and a reliable noise theory has not been developed at the time, to our knowledge. However, in the other FET devices we recognize three sources of noise: thermal noise, due to inherent resistive components of the structure; shot noise, resulting from charge crossing a potential barrier; and contact or flicker noise, also referred to as $1/f$ noise, which results from traps at interfaces. These interfaces are typically metal/semiconductor junctions, heterojunctions, etc. and contact noise is predominantly a low frequency phenomena. The noise sources can manifest themselves as voltage or current noise. For a FET the voltage noise is given as

$$22) \qquad e_n^2 = 4KT\frac{2}{3g_m} + K_2\frac{I_D^a}{g_m^2 f}$$

where K_2 is a constant and the exponent "a" takes on a value between 1/2 and 2.0. The first term represents thermal noise and the second $1/f$ noise. Both noise sources are reduced for large transconductance, g_m. The current noise is given as

$$23) \qquad i_n^2 = 2qI_g + \left(\frac{2\pi f C_{g_s}}{g_m}\right)\left(4KT\frac{2g_m}{3} + K_3\frac{I_D^a}{f}\right)$$

The second term in Eq. (23) is a restatement of Eq. (22) in terms of current whereas the first term represents shot noise. For an ordinary FET this is expressed as dependent on the gate current due to charge crossing the Schottky barrier. In a HEMT structure there may be other sources shot noise associated with charge crossing the various heterojunctions between the layers of the wafer. Finally, the noise figure for a HEMT is given as [22]

$$24) \qquad NF_{\min} \cong 1 + 2\omega\frac{C_{g_c}}{g_{m_0}}\left(\frac{R_s + R_g}{R_i}\right)^{1/2}$$

where g_{m_o} is the intrinsic transconductance, C_{g_c} is the gate-channel capacitance, R_s is the source resistance, R_g is the gate resistance, and R_i is the input or channel resistance. In essence, Eq. (24) tells us we want low source resistance and high cutoff frequencies to achieve low noise.

From these considerations of possible noise sources it was decided that wafers 3-1603, 3-1605 and 3-1800 be processed. Wafer 3-1599 was not recommended for processing because we believed that the channel was too narrow (130 Å) and may be subject to higher shot noise as the electrons concentration at the barrier on the substrate side of the channel was significantly greater

than in the other structures. In effect, we felt the electrons in the channel may have been over confined.

V.3. INVESTIGATING FACTORS INFLUENCING HEMT PERFORMANCE

While Martin Marietta was processing the three preliminary wafer structures, SRA initiated a computational investigation. This investigation employed one- and two-dimensional simulations of a basic HEMT structure and then introduced parametric variations in the structure. The effects of these changes on device performance were then evaluated to gain insight towards the optimum design of the 0.1 μm gate HEMT device.

V.3.1. Reference Device, Structure

Our reference device structure is shown in Fig. 9 and is similar to the structure used in the Phase I research effort. A 100Å narrow band gap cap layer doped to $2x10^{18}/cm^3$ sits on a 200Å gate isolation layer of an undoped wide band gap material. The gate is recessed 100Å into this layer. The planar doped layer is modeled as a 10Å thick layer doped to $5x10^{19}/cm^3$ yielding a planar doping of $5x10^{12}/cm^2$. This layer is separated from the channel by 30Å of the wide gap material. The channel is an undoped narrow gap material, 800Å wide and sits on a 0.25 micron wide gap buffer. The entire structure is grown on a suitable substrate (not shown).

V.3.2. One-Dimensional Results

Prior to performing 2-D simulations of the complete HEMT to obtain the performance variation due to parametric alterations of the structure, we performed 1-D simulations to investigate how the variations alter the nominal charge distribution under the gate. We begin by noting that if there were no mobile charge between the gate surface and the edge of the channel, the capacitance of this layer would be given as

$$25) \quad C_g = \frac{\varepsilon A_g}{t}$$

where A_g is the gate area (length time width) and t is the thickness of the material between the gate and the channel. Since

$$26) \quad t = t_{recess} + t_{spacer}$$

where t_{recess} is the thickness of the material between the gate surface and the planar doped layer, and t_{spacer} is the spacer layer thickness, we except C_g to increase if either the gate recess depth is increased (decreasing t_{recess}) or the spacer layer thickness is reduced or both. Equations (25) and (26) suggest that the gate capacitance is unaffected by the gate bias level. However, this is not the case as the mobile charge in the channel introduces a series capacitance which is modulated by the gate bias. Equations (25) and (26) provide only an indication of how we expect the C_g to vary with

t_{recess} and t_{spacer}. Given an estimate of the capacitance we also note that the charge in the 2-DEG in the channel is given approximately as

$$27) \qquad n_g = \frac{(V_g - V_T)C}{eA_g}$$

where V_g is the applied gate bias and V_T is the threshold voltage.

Between Eqs. (25, 26 and 27) the effects of device geometry are accounted for but the effects of the planar layer doping level do not explicitly appear. As we shall see, variations in the planar layer doping level affect the charge sheet density and capacitance in such a way that they can be accounted for by a change in V_T. Thus, over a good portion of the operating range, both C_g and n_g collapse onto a single curve when expressed as

$$28a) \qquad C_g = f(V_g - V_T)$$

$$28b) \qquad n_g = g(V_g - V_T)$$

V.3.2.1. Results for the Reference Structure

The first series of simulations performed were for the reference structure shown in Figure 9 in a plane normal to the center of the gate contact. The distance from the gate recess to the planar doped layer was 100 Å and the spacer layer thickness was 30 Å. The planar doped layer was 12 Å

wide and doped to $5x10^{19}/cm^2$ or a charge sheet density of $6x10^{12}/cm^2$. The channel was 800 Å wide. The results of the simulations based on quantum hydrodynamics equations are shown in Fig. 10 where the electron density distribution, charge sheet density of the 2-DEG and capacitance derived from the sheet density are shown as a function of gate bias. Here the capacitance is computed as the derivative of the total charge in the structure with respect to gate bias. The gate surface is at 0.02 μm and the channel begins at 0.033 μm. From Eq. (25) we would expect the capacitance to be in the range of 0.047 pf for a $0.1x50\ (\mu m)^2$ gate. From Fig. 10c we see that this value is in agreement with the results at a gate bias of 0.4 volts. However, at lower bias levels the capacitance drops below this value significantly and nonlinearly as the mobile charge in the 2-DEG is modulated. Equation (25) provides an estimate of the *maximum* capacitance.

For this case we found the threshold voltage to be approximately -0.34 volts. Using the capacitance value of 0.047 pf from Eq. (25) and the threshold voltage above yields the dashed curve in Fig. 10b, from Eq. (27) which overpredicts the charge sheet density. Thus, while Eqs. (25) and (27) give an estimate of capacitance and charge sheet density we can expect under the gate, they also introduce significant errors.

V.3.2.2. Reduced Planar Layer Doping

The next case considered was for the same structure but with a 20% reduction in the planar layer doping. We immediately note the expected reduction in the peak electron concentration and the reduction in the charge sheet density shown in Fig. 11a and b. Also evident is the reduction in the capacitance shown in Fig. 11c. Equation (25) states that the capacitance for this structure

should be the same, but this would be true only in the absence of mobile charge. The threshold voltage for this case, from Figure 11b, is found to be -0.2 volts and again, Equation (27) yields a similar estimation of the charge sheet density of the 2-DEG.

The observation of these two cases presents an important result. If we transform the x-axis from $x = V_g$ to $x' = V_g - V_T$ and plot the results for charge and capacitance we see that the results for these two cases collapses onto each other, as shown in Fig. 12. Thus, we can conclude that even though these two structures are different, their performance should be very similar with the exception of the threshold voltage. The difference in planar layer doping will also affect the source-gate and gate-drain resistance and this may have an effect on the noise performance of the device.

V.3.2.3. Effect of Gate Recess

The next device modification considered is that of increasing the gate recess depth. This is of interest because during processing it may be difficult to control the gate recess depth. In the case considered here we have exaggerated the variation in the recess depth to provide a clear picture of the associated effects. Figure 13 shows the results for a gate recess of 150 Å, a 50% increase from the initial case presented in Figure 10. Due to the closer proximity of the gate to the 2-DEG in the channel we would expect greater control and higher capacitance as indicated from Eq. (25). Figures 13a and 13b show that the electron density and charge distribution in the channel undergo greater modulation for the same swing in gate bias. Due to the smaller distance between the gate and channel it is also necessary to forward bias the gate by approximately and additional 0.2 volts, compared to the original structure to reach a sheet density of the order of $2.7 \times 10^{12}/cm^2$.

Equation (25) yields a capacitance of 0.077 pf for the structure which is well above that obtained from the variation of the charge sheet density with bias. However, it still provides an estimate of the maximum capacitance to be expected.

V.3.2.4. Effect of Spacer Layer Thickness

When the spacer layer thickness is increased from 30 Å to 45 Å, the results are as shown in Fig. 14. The gate recess is 100 Å as in the original structure. The increase in spacer layer thickness reduces the gate capacitance. Also evident in the result is the presence of residual charge in the planar doped layer. The conduction band discontinuity is too far away from the planar doped layer to fully deplete it. The capacitance from Eq. (25) again yields a maximum value of 0.042 pf, in good agreement with that obtained from the sheet density at 0.4 volts.

V.3.2.5. Effect of Channel Depth

The last series of one-dimensional calculations were performed for a device in which the channel depth was decreased from 800 Å to 200 Å. According to Eqs. (25 and 26) we would not expect any significant changes in the properties of the electron distribution under the gate. Figure 15 shows that this is indeed the case. The electron density profiles show the effect of greater confinement but the charge sheet density and capacitance are almost identical to the results shown in Fig. 10 for the original structure. The greater confinement would lead us to believe that the

device will have harder saturation characteristics than the original structure. This will require a two-dimensional simulation to determine the degree to which the I-V characteristics change.

The results presented here show that the estimate of capacitance and charge sheet density given by Eqs. (25-27) provide upper limits when compared to one-dimensional simulations. The observation that the capacitance is not constant over the bias range investigated is a reflection of the mobile charge in the channel. As the gate bias is reduced, the charge is depleted. This then introduces a series capacitance and results in a reduction in capacitance. Additionally, the fact that there is only a finite amount of charge in the channel which can be depleted limits the linearity of the capacitance and charge vs. gate bias relationship.

V.3.3. Two-Dimensional Results

While the previous one-dimensional analysis is useful to provide estimates of the characteristics of the charge under the gate in a quantum well HEMT, we must still address how well these relate to the actual two-dimensional structure. To do this we have performed full two-dimensional simulations of the reference structure of Fig. 9 and of the variants.

V.3.3.1. Results for the Reference Structure

The predicted current-voltage characteristics for the reference structure are shown in Fig. 16. These results show moderately hard saturation in the I-V curves indicating good isolation and confinement of charge in the channel. Figure 17 shows the variation of the transconductance, the

capacitance and the cutoff frequency as a function of gate bias at V_{ds} = 1.0 volts. At V_{gs} = 0.2 volts the transconductance is 705 ms/mm, the capacitance is 0.0387 pf and the cutoff frequency is 144.7 GHz. We note that the values of capacitance are in reasonable agreement with the simple one-dimensional simulations although the variation is more linear. This is because in the two-dimensional case the 2-DEG to the source and drain sides of the gate contribute to the charge in the gate depletion region. These "edge effects" increase the capacitance over the one-dimensional values, particularly at lower gate bias where there is more depletion directly under the gate than toward the edges. This is shown in Fig. 18 where the charge sheet density vs. distance along the channel is shown for V_{gs} = 0.2 volts and V_{ds} = 1.0 volts. The nominal level of the sheet density is in agreement with the one-dimensional result (Fig. 10b) but at the source edge of the gate we see the sheet density is considerably higher. We are also able to calculate the transconductance and cutoff frequency directly from the two-dimensional results. It is possible to estimate the transconductance as

$$30) \qquad g_m = \frac{V_s C_g}{A_g}$$

where V_s is the saturation velocity under the gate and obtain a value for g_m from the one-dimensional results. However, this approximation is only as good as the estimates of C_g and V_s. On the other hand, we can determine V_s from Eq. (30) and the results from the two-dimensional simulations. At V_{gs} = 0.2 and V_{ds} = 1.0; this yields $V_s = 0.9108 \times 10^7$ cm/sec. It is also possible to estimate V_s from the drain current and the charge sheet density:

31) $$V_s = \frac{I_d}{qn_g W_g}.$$

Equation (31) yields a saturation velocity of 1.25×10^7 cm/sec. The discrepancy between Eq. (30) and Eq. (31) arises because Eq. (30) is simply an expression of the cutoff frequency in terms of a velocity and the gate length

32) $$V_s = 2\pi f_t \ell_g$$

whereas Eq. (31) is an exact expression which depends only on the accuracy of the measurements or predictions of I_d and n_g. From Fig. 10c and Fig. 17, at $V_g = 0.2$ volts the capacitance is seen to be in good agreement between the one- and two-dimensional results. Thus, we would expect the estimate of V_s from Eq. (31) using the one-dimensional charge sheet density to be in good agreement with the two-dimensional result. This is indeed the case as the two-dimensional charge sheet density and the saturation velocity computed from Eq. (31) as a function of position along the channel and shown in Figs. 18 and 19 reveal. We emphasize that this velocity is an average value across the channel and does not represent local maximums which may include velocity overshoot effects. Such effects shall be discussed subsequently when we examine the detailed transport in the device.

V.3.3.2. Reduced Planar Layer Doping

As with the one-dimensional simulations we now investigate the effect of a 20% reduction in planar layer doping. While this is a significant variation, it is not too large to be considered unrepresentative of process variations, yet it is large enough to provide a clear indication of the effect of such variations on device performance.

The I-V characteristics for this device are shown in Fig. 20. Here we observe an overall reduction in the current levels, as would be expected, due to reduced conductivity in the channel. The lower planar layer doping leads to a lower density in the 2-DEG. The saturation shown in the I-V characteristics is also slightly harder. The transconductance, capacitance and cutoff frequency as a function of gate bias for V_{ds} = 1.0 volts are shown in Fig. 21 for this device. We note a significant reduction in the transconductance in this structure and greater variation with gate bias. At V_{gs} = 0.2 volts g_m is 587 ms/mm compared to the value of 705 ms/mm for the initial structure, the capacitance is 0.0350 pf compared to 0.0387 pf, and the cutoff frequency is 133.5 GHz compared to 144.7 GHz. We note that the lower value of f_t arises since g_m decreases faster than C as the planar layer doping is reduced. The transconductance varies more rapidly with gate bias because the device is closer to pinch-off.

The reduction in transconductance with lower planar layer doping is an important result. It has been argued that in such structures the gate isolation layer is similar to the oxide layer in a MOSFET and, as a result, the transconductance should behave, with variation in planar layer doping, similar to that observed with doping variations of the channel in a MOSFET. However, there are important differences between the two structures. In a MOSFET the capacitance of the

oxide layer is fixed by the oxide thickness and the conduction in the channel is based on inversion. The transconductance is directly proportional to this capacitance and, as given in [22] for an idealized MOSFET, will increase slightly as the doping under the oxide is reduced. However, in the present structure the capacitance under the gate is not constant. The charge from the planar doped layer is distributed in the 2-DEG in the channel and is modulated with the gate bias. The behavior is thus similar to a MESFET and, as noted, the transconductance decreases as the planar layer doping is reduced.

When we compare these results with the one-dimensional results we again note the reasonable agreement for the capacitance presented in Figures 11 and 19 for gate bias levels above 0.2 volts. Below this value the one-dimensional result again drops off faster.

V.3.3.3. Effect of Gate Recess Depth

We recall from our one-dimensional simulations that the increase in the depth of the gate recess from 100 Å to 150 Å resulted in greater modulation of the charge sheet density with gate bias and higher capacitance. We also expected greater control of the device, which should be reflected by an increase in the transconductance, and lower currents overall due to the greater depletion resulting from the reduced spacing between the gate and the channel. The predicted I-V characteristics shown in Fig. 22 are in agreement with this expectation. The current levels are significantly below that of the original structure, and even below that of the structure with reduced planar layer doping. A forward bias of 0.6 volts is required at the gate to obtain current levels previously obtained with $V_{gs} = 0.4$. However, as shown in Fig. 23 above $V_{gs} = 0.2$ the

transconductance of this variation of the original device is higher, and shows a significant variation with V_{gs}. The capacitance, while initially lower, also shows greater variation and rises above that of the original structure for V_{gs} greater than 0.2 volts. These results are further reflected in the cutoff frequency. Due to pinch-off effects at $V_{gs} = 0.0$, the cutoff frequency at low gate bias is significantly below that of the original structure. As V_{gs} is increased, the transconductance increases faster than the capacitance, and f_t increases. Between $V_{gs} = 0.2$ and $V_{gs} = 0.4$, f_t is relatively constant at about 144 GHz to 145 GHz. Above $V_{gs} = 0.4$, f_t begins to drop to a value of 138 GHz. Overall, however, the cutoff frequency is above that of the original structure for V_{gs} greater than 0.2 volts. These results indicate that if an increase in the threshold voltage is acceptable, a slight increase in high frequency performance may be obtained by increasing the depth of the gate recess. However, there is some sacrifice of linearity and the closer proximity of the gate contact to the active channel may adversely affect the noise performance.

V.3.3.4. Effect of Spacer Layer Thickness

From the results of the one-dimensional studies we expect an increase in the spacer layer thickness to result in lower currents, capacitance and transconductance. This is due to the lower charge sheet density in the channel and the weaker control of the channel charge since the gate is further away. As shown in Figs. 24 and 25 the two-dimensional results for a device with a 45 Å spacer layer confirm this. The current levels are reduced significantly from those of the original device configuration in which the spacer layer was 30 Å. While both the capacitance and transconductance are reduced, the rate of decrease is not equal, thus f_t decreases for this structure.

We also note that the transconductance decreases slightly with increasing gate bias. At $V_{gs} = 0.2$ $g_m = 550$ ms/mm, $C = 0.0353$ pf and $f_t = 124$ GHz.

V.3.3.5. Effect of Channel Depth

Continuing to follow the path of the one-dimensional investigation we finally consider the effects of a decrease in channel depth from 800 Å to 200 Å. The one-dimensional results indicated greater confinement but with little change in capacitance from the original structure and suggested harder saturation. The two-dimensional results bear this out. Figure 26 shows a comparison of the I-V characteristics for this structure and the original structure. The current levels are clearly very nearly the same with the narrow channel results showing the expected harder saturation. However, the capacitance of the structure, shown in Fig. 27, is significantly different from that of the original structure and shows a departure from the one-dimensional result. At high gate bias level the capacitance is slightly higher than that of the original structure, shown in Fig. 17. As the gate bias is decreased, the capacitance decreases much more significantly to a value of 0.03 pf compared to 0.0355 for the original structure. Differences are also found in the transconductance which shows a marked decrease with increasing gate bias. The original structure has almost constant transconductance. The effect of these changes yields a cutoff frequency which also varies widely with gate bias. At $V_{gs} = 0.0$ volts, a cutoff frequency of 194 GHz is obtained, but at $V_{gs} = 0.4$ volts, the cutoff frequency drops to only 112 GHz. Such significant differences between the two structures were not anticipated from the one-dimensional investigation.

V.3.3.6. Effect of Cap Layer Doping

The final two-dimensional simulation is for a structure similar to the original structure but with undoped cap layer. From the one-dimensional vantage point this device appears identical to the original structure with respect to the distribution of charge under the gate. The question then arises as to whether or not any significant differences will be revealed in the two-dimensional simulations. Experimentally, [7], differences in the degree of saturation in the I-V characteristics was observed as well as an increase in MSG compared to a surface doped structure. While the device in [7] was not identical in structure to that simulated here it is similar enough that we would expect a similar result. The observed result was attributed to a surface-induced field spreading effect in the region between the gate and the drain. The effect can only be investigated using two-dimensional simulation.

The current-voltage characteristics for the simulated devices with and without doping of the cap layer are shown in Fig. 28. We note that there are no significant differences in this comparison. Figure 29 shows transconductance, capacitance and cutoff frequency obtained for the undoped cap layer device. The transconductance shows a greater variation with gate bias than the structure with a doped cap layer (Fig. 17). This is a small difference, however, and reflects the sensitivity of the transconductance to small changes in the drain current. The transconductance is nominally in the 700 ms/mm range, as was the original structure. Differences in the capacitance, shown in Fig. 29b, are more significant and are a result of the reduction of the overall level of charge in the device. It should be noted, however, that while the cap layer is undoped, there is still substantial accumulation of charge in the cap layer due to the heterojunction present at the interface between the cap layer

and the Schottky enhancement layer. Finally, the cutoff frequency shown in Fig. 29c reveals a slightly higher result at increasing bias level. In general, though, the undoped cap layer shows very little effect on performance. At $v_{gs} = 0.2$ volts and $V_{ds} = 1.0$ volts $g_m = 711$ ms/mm, $C = 0.0374$ pf and $f_t = 151.3$ GHz.

In view of the experimental results of [7] we must ask why we do not see significant variations in performance when the cap layer is undoped. If we examine the potential distribution for the two devices, as shown in Fig. 30, we see no meaningful differences in them. In [7] differences in performance are attributed to a surface field spreading effect. We do not observe this effect. The 2-DEG in the channel maintains a relatively uniform field in regions between source and gate, and the gate and drain. Additionally, the heterojunction between the cap layer and the enhancement layer, and the enhancement layer and the channel have the major effect on determining the density level in the 2-DEG and in the cap layer. In [7] simulations which revealed the surface field spreading effect did not include the cap layer. In the undoped cap layer simulation the distance between the edge of the gate recess and the drain contact was altered and the enhancement layer was exposed. While this may account for the difference in the simulation results, it does not account for the difference in performance observed experimentally. We believe that the difference observed experimentally may be associated with contact formation since our contact model was unaltered in the two structures.

V.4. DETAILED CHARACTERISTICS OF TRANSPORT IN HEMTS

The internal characteristics of the transport within the reference HEMT structure are present in this section. The characteristics are qualitatively similar for all devices of this basic structure. Our initial simulations using a planar doped layer proved difficult in the two-dimensional case. These problems were related to convergence of the two-dimensional numerical procedure. To circumvent these convergence problems the structure was initially modified. The AlInAs gate isolation layer was doped. It was noted in [7] that through penetration of the metalization of the source and drain direct contact to the 2-DEG in the channel was achieved. The contacts were, as a result, ohmic with a reported resistance of approximately 0.3 Ω·mm regardless of the doping of the cap layer. Thus, it would appear that the interfaces between the InGaAs cap layer, the AlInAs isolation layer and the channel were obliterated. Electrons could easily enter and exit the channel under the contacts as a result. However, away from the source and drain metalizations the heterojunctions would remain intact providing the desired isolation. In our simulations we have modeled this by elimination of the variations in the band gap between the various layers in the region of the source and drain and by extending the N^+ doping levels into the channel to mimic penetration by the metal. Without this modification, even with quantum corrections included in the governing equations, it was not possible to inject significant charge into the 2-DEG due to the barrier created by the gate isolation layer.

Typical results for this structure are shown in Figs. 31-34 for a bias of $V_{DS} = 0.75$ and $V_{gs} = 0.4$ volts. In Fig. 31 surface plots of the electron density, (a), potential (b), and electron, temperature (c), are shown across the first 2000 Å of the device depth. The outline of the device

structure is shown below the temperature surface for reference to later figures in which profile plots normal to the contact surface are presented. While the details of the distribution of electrons and potential are difficult to see in Fig. 31, the results do show interesting qualitative effects. We observe from the density surface the uniform contours under the source and drain resulting from the modeling of the metalization of the contacts, as discussed earlier. The potential surface also reflects this and the result is a low resistance ohmic contact to the 2-DEG in the channel. As we move away from the source or drain, towards the gate, an increase in electron concentration is observed with a sharp peak in the N^+ cap layer. Also, as a result of the applied drain bias we note the presence of a small field in the source-drain direction between the edge of the gate recess and the drain. This results in a lower electron density near the drain side of the gate recess as compared to that on the source side of the recess. While this will have little influence on the D.C. characteristics of the device, due to the function of the gate isolation layer, it will affect transient behavior. This "sloshing" of charge with bias level will affect the parasitic capacitance of the device. Near the source side of the gate recess we observe the presence of a second peak in the electron density. This peak is lower and is associated with the peak in the charge density in the 2-DEG in the channel. The peak runs the entire length of the channel, except at the source and drain regions, but cannot be clearly seen in this plot. The depletion of the 2-DEG under the gate is clearly evident in the results.

The electron temperature shows a sharp peak near the drain end of the gate. Over most of the device the electrons are near equilibrium with the lattice. However, as the electrons accelerate in the low density region of the 2 DEG under the gate the temperature rises. The maximum temperature reaches approximately 600°K and occurs in the high field region just to the drain side

of the gate. In this region the electrons slow down as they enter a high density region of the 2-DEG gas. The kinetic energy of the electrons is dissipated as heat in this region. As the electrons continue to decelerate, the temperature relaxes back to nearly the lattice temperature.

Due to the difficulty in deciphering the details of the solution from Fig. 31, we present profile plots of the same results in Figs. 32-34 along the lines marked on the projection of the device shown in Fig. 31. Figure 32 presents profiles of the electron density on both a linear (a) and log (b) scale. The curves labeled A&E in Fig. 32a show the electron density under the source and drain contacts. We note the penetration of the doping into the channel allowing direct contact to the 2-DEG. The curve labeled B shows the profile on the source side of the gate recess while curve D is on the drain side. Here we observe that the electron density in the channel has a similar peak level but electrons are drawn away from the substrate on the drain side due to the applied bias. We also note the higher peak density in the cap layer is on the source side of the gate recess, as discussed previously, due to the small source-drain direction field in this layer. Curve C represents the profile under the gate. We note here the significant depletion of the 2-DEG under the gate, even with a forward bias of 0.4 volts. Figure 33 shows the potential profiles at the same locations. The constant potential regions under the source and drain (A&E) again indicate low resistance contact to the 2-DEG in the channel and the peaks in potential curves (B&D) are a result of depletion of the charge in the isolation layer. Finally, profiles of electron temperature are shown in Fig. 34. Here we observe that under the source and drain the electrons are close to being in equilibrium with the lattice (A&E). The maximum heating occurs on the drain side of gate (C), and the temperature then begins to relax back to the lattice temperature (D).

Having gained experience with our two-dimensional algorithm through simulation of the modified HEMT structure we returned to the original structure with an undoped 200 Å layer of AlInAs, and a planar Si doped layer (assumed to be 10 Å thick and doped to $5x10^{19}/cm^3$). The region under the source and drain contacts was treated as in the modified structure except that the doping under the contacts was raised to $1x10^{19}/cm^3$. Our initial result was to compute the zero bias solution to establish the 2-D electron gas in the channel. We also computed a classical zero bias solution for this structure as a reference. The results for the density distributions are compared in Figs. 35 and 36. Figure 35 shows a comparison of the classical and quantum corrected density distributions in the direction normal to the device surface, through the channel and extending slightly into the AlInAs buffer layer. The distributions lie in a plane passing through the device half-way between the source contact and the gate recess. Here we note that the classical solution yields higher peak densities and sharp, abrupt interfaces. The peaks are located at the material interfaces. In comparison, the quantum corrected result shows a continuous density distribution with the peaks reduced in magnitude and shifted away from the interfaces, and a reduction in the depth of the depletion of the planar doped layer. Both results show an initial peak in the InGaAs cap layer at or near the interface with the gate isolation layer. The second peak occurs in the region of the planar doped layer. Recall that this layer is modeled as a 10 Å wide layer. It is doped to $5x10^{19}/cm^3$ to yield the desired planar density of $5x10^{12}/cm^2$. This layer is heavily depleted. The carriers depleted from the planar doped layer seed the channel and provide the mobile charge for the 2-DEG which is represented by the third peak. Some of the depleted carriers accumulate in the cap layer yielding the peak observed there. With the exception of the region near the interface between the spacer layer and the channel, the charge distribution across the channel is very similar

for both calculations. At the interface between the channel and the buffer layer, we again observe some differences arising from the quantum effects at this abrupt junction. We must also emphasize that these results are on a log scale. The peak densities in the 2-DEG are significantly different. In the quantum corrected result the peak is $7.4x10^{18}/cm^3$. In the classical case the peak density is nearly four times greater at $2.9x10^{19}/cm^3$. However, the total charge in the channel is not altered to as great a degree due to the broader nature of the quantum mechanical distribution. The major significant difference is the level of charge in the spacer layer. Here the classical result shows almost a complete absence of charge whereas the quantum corrected result yields a minimum density in this region of $1.5x10^{18}/cm^3$. This is clearly a significant level of charge and will contribute to conduction in the device. We also note the quantum corrected density distribution reflects a continuous variation in the conduction band energy (including Q) while the classical result reflects the discontinuities associated with the barriers at the material interfaces. The quantum potential is responsible for this as it always tends to smooth out these discontinuities.

Figure 36 shows a similar comparison for a plane dissecting the device normal to the gate contact. We observe the continuous variation in density in the quantum result, increasing from the gate to a peak of $3.2x10^{18}/cm^3$ in the 2-DEG, then decreasing across the channel until reaching the interface with the buffer layer. The classical result exhibits a double peak structure and still clearly reflects the presence of the planar doped layer. The higher peak associated with the 2-DEG is at $1.08x10^{19}/cm^3$. At the gate surface the density is approximately two orders of magnitude greater in the quantum corrected solutions. This is consistent with a lowering of the barrier height by the quantum potential.

The peak density in the 2-DEG is lower in the quantum corrected result than in the classical result. In fact, if we examine a plane parallel to the device surface passing through the peak density in the 2-DEG from source to drain, the quantum corrected distribution shows a significantly lower peak than the classical result along the entire length of the channel.

Surface plots of the equilibrium density and potential distributions are shown in Fig. 37. Recall that the doping under the contacts has been raised to $1x10^{19}/cm^3$ to give a better representation of the metalization. A wire mesh plot is presented for the potential since it reveals details behind the 2-DEG. It also shows the mesh structure which consists of 107 X points by 136 Z points. We observe in the density plot that the 2-DEG does not extend completely into the contact regions. This is a result of a grading, in the source-drain direction, of the barriers associated with the interfaces between the InGaAs cap layer and channel, and the AlInAs gate isolation layer. This grading is introduced, as previously discussed, to represent the obliteration of these interfaces by the metalization. These barriers, and as a result the 2-DEG, are well established before the active gate region of the device is reached. No grading was introduced in the direction normal to the barriers. We also note that as we traverse from the source to the gate there is an increase in the peak density of the 2-DEG in the region of the gate recess. The same effect is also apparent on the drain side of the device. This is a direct result of the gate recess and the absence of the barrier between the cap layer and the isolation layer which is present away from the gate recess. Away from the recess, carriers depleted from the planar doped layer accumulate in both the cap layer and the 2-DEG. The carriers that accumulate in the cap layer are responsible for the first peak shown in the density distribution of Fig. 35. Under the gate recess, carriers from the planar doped layer can accumulate only in the 2-DEG. This has the two-fold effect of increasing the 2-

DEG density and reducing the level of depletion of the planar doped layer in the region. Directly under the gate contact the peak density is reduced due to depletion by the Schottky barrier.

The potential surface reveals a large rise in potential from the source extending to the drain where it returns to the same level as at the source. This spike in potential is associated with the depletion of the planar doped layer and establishment of the 2-DEG in the channel. Under the gate recess the slight increase in potential is a result of the higher density of the 2-DEG discussed previously. The presence of the gate contact is apparent in the lower potential in the depletion region.

Figure 38 shows an enlarged wire mesh plot of the quantum potential for this case. The region shown in the figure extends from an area just to the source side of the gate recess to the center of the gate contact. The region extends only slightly into the channel. At the left end of the figure we see a one-dimensional distribution of the quantum potential exists from the device surface into the channel. The quantum potential is zero at the device surface and decreases to a local minimum at the interface between the cap layer and the gate isolation layer. Across the interface, in the AlInAs, a maximum is reached. This quickly decays to zero, then after a dip in the region of the planar doped layer, the quantum potential rises to a second maximum on the AlInAs side of the interface with the channel. Crossing the barrier into the channel we observe a second minimum on the InGaAs side of the barrier which quickly decays to zero. We also note that the length scales over which the quantum potential varies are consistent with our analysis and are on the order of tens of angstroms.

In the region of the gate recess, we see that the quantum potential still behaves one-dimensionally. The recess itself does not alter the distribution significantly. However, as we

approach the gate contact from the side, we observe a rapid rise in the quantum potential. The same effect is noted as we approach the gate in the direction normal to the gate surface. This is because the Schottky contact represents another barrier which the quantum mechanical effects try to lower. The effects are highly localized and have little influence on the distribution of the quantum potential at the channel interface. A slight increase in the quantum potential in the region of the channel interface is noted as we move in the source to drain direction, but this is not significant compared to the variations normal to the surface.

When a bias is applied to the structure the distribution of density, potential, velocity along the channel, and temperature appear as shown in Fig. 39. This result is for the case of $V_{ds} = 0.5$, and $V_{gs} = 0.4$ volts. The most pronounced effects observed in the density surface are the increase in the density at the source side of the gate recess, the distortion of the depletion region with lower density at the drain end of the gate and the reduction of the density peak on the drain side of the gate recess. These three effects are all the result of the gate recess and the applied bias. As a result of the constriction caused by the gate recess, additional electrons accumulate on the source side of the gate in this region. They accumulate there because they are about to enter the high resistance region under the gate. Directly under the gate the electrons accelerate, further reducing the density in the 2-DEG. This effect is typical of the depletion under a Schottky contact. To the drain side of the gate, the peak in the 2-DEG caused by the gate recess is eliminated because the electrons in this region are quickly drawn away along the highly conductive path to the drain.

The potential distribution reflects these effects and shows that relatively uniform fields exist along the 2-DEG. The field in the cap layer, on both sides of the gate recess, is nearly zero. The small fields which do exist in the cap layer in the source-drain direction balance a small

accumulation of charge on the source side of the gate recess and depletion on the drain side. This result is similar to that of our preliminary device structure. We reiterate that the sloshing charge in the cap layer will affect the parasitic capacitance of such devices. Under the gate we observe that the potential rises to a higher value than in our preliminary structure. This is a direct result of the increased density of the 2-DEG when the planar layer is correctly modeled. The total density of dopants in the isolation layer is nearly the same in both cases, $4x10^{12}/cm^2$ in the preliminary structure and $5x10^{12}/cm^2$ in the real structure. However, due to the proximity of the planar doped layer to the channel, most of the charge seeds the 2-DEG whereas in the preliminary structure most of the charge accumulated in the cap layer. Additionally, since the isolation layer is only 100 Å thick under the gate recess, only half as much charge was available to seed the 2-DEG in the preliminary structure. Thus, as is evident from the density surface plot, the channel is much more highly conductive when the planar layer is correctly simulated.

Figure 39 also shows surface plots of the velocity along the channel and the electron temperature. The velocity surface shows the acceleration of electrons as they enter the 2-DEG. Between the source and gate, and the gate and drain the electron velocity is almost constant in the 2-DEG. As we move across the channel into the buffer layer, the velocity shows a smooth increase and then a smooth decrease moving from source to drain. Directly under the gate we observe a rapid acceleration in response to the lower density arising from the gate depletion layer. A peak in the velocity occurs at the drain end of the gate contact. The peak approaches $1.35x10^7$ cm/sec. While difficult to see in this figure, the velocity in the cap layer is zero. An indication of this is apparent at the source end of the figure.

Finally, we examine the electron temperature surface. Here we note a minor cooling of electrons as they enter the 2-DEG. This results because of an exchange of thermal energy to kinetic energy in this region. The thermal response lags the acceleration spatially. The effect is short lived, however, and the electrons then rise slightly in temperature in the established region of the 2-DEG. The electron temperature rises considerably under the gate. Upon reaching the drain end of the gate they then decelerate, cool and maintain a constant temperature until they reach the drain. The maximum temperature under the gate reaches 340°K at this bias level. Upon further deceleration, as the electrons exit the 2-DEG and arrive at the drain, an inverse of the effect observed at the source is shown. Here the excess electron kinetic energy is initially converted to thermal energy as the deceleration begins and the temperature rises slightly. As the electrons continue to slow, the temperature relaxes to the lattice temperature. The peak temperature is lower than in the preliminary structure because of the greater conductivity of the channel.

The electron velocity and temperature variations in the plane of the peak density in the 2-DEG are shown in Fig. 40 at the same bias condition. Here we can clearly observe the acceleration of electrons from the source region into the 2-DEG where the velocity is near 0.6×10^7cm/sec. The slight dip in the velocity is in the region where the density increased due to the beginning of the gate recess. The electrons then accelerate sharply as they enter the gate depletion region. A final rapid acceleration to 1.35×10^7cm/sec occurs in the region of minimum density and maximum electric field. The electrons then decelerate to a level somewhat below 0.6×10^7cm/sec. A slight acceleration occurs just before the electrons decelerate at the drain metalization.

The temperature distribution shows clearly the initial drop below 300°K as the electrons enter the 2-DEG. Once in the 2-DEG the temperature rises to 310°K. The electron temperature

continues to rise to about 315°K before encountering the region under the gate. Here the temperature peaks at 340°K. The electrons then cool as they approach the drain. The minimum in temperature and slight rise before cooling in the drain region coincide with the small velocity peak and initiation of deceleration just before the drain is reached.

When the drain bias is increased the distributions of potential, density, velocity, etc. are qualitatively similar. Higher velocities and temperatures occur under the gate, and there is deeper depletion at the drain edge of the gate. As an example of such results we present the potential distribution at V_{ds} = 1.5 volts and V_{gs} = 0.4 volts in Fig. 41. We note that the distribution of potential on the source and drain sides of the gate is almost identical to that at V_{ds} = 0.5 volts due to the high conductivity of the 2-DEG. Most of the increase in potential is applied to overcome the high resistance region at the drain side of the gate. The velocity reaches a peak value of 1.41×10^7 cm/sec and the temperature reaches 365°K in this region.

V.5. EXPERIMENTAL RESULTS FOR PRELIMINARY STRUCTURES

To investigate various wafer structures for lower noise and higher speed, different InAs compositions in the channel were studied. These consisted of four InP HEMT wafer pieces grown at the Martin Marietta Laboratory with InAs mole fractions of 0.60, 0.65, 0.70 and 0.75. The channel thickness of the material was designed to allow a stable pseudomorphic structure. The four wafer structures are shown in Figs. 42 to 45. The relative variation of the charge sheet density of these structures was consistent with the one-dimensional wafer analysis discussed previously with the exception of the 75% mole fraction wafer (wafer No. 1599). This wafer had an unexpected low

sheet density which was possibly due to either the very thin channel thickness (130 Å) or non-optimized growth of the layer. The one-dimensional simulations did not reveal this behavior, thus the growth process is thought to be the more likely cause.

As a result of the noise consideration discussed earlier, and the poor sheet density of wafer 3-1599, only three wafer structures were processed: wafers 3-1603, 3-1605 and 3-1800, for HEMT production. Two pieces from wafer 3-1599 were processed as dummies to test for gate exposure. The wafers were processed using Martin Marietta Electronic Laboratory's established InP HEMT all E-beam lithography wafer process. The device layout is similar to the InP HEMTs used in the Phase I study and is shown in Fig. 46. The HEMT has a T-gate with a 0.1 μm length and a 30 μm width for a good impedance match at 94 GHz.

A strong oscillation in current was observed during the preliminary DC testing of these wafers, making data recording very difficult and time consuming. However, it was possible to obtain the DC I-V characteristics of these three devices. Results for wafer 3-1603 are shown in Fig. 47, those for 3-1605 in Fig. 48 and those for 3-1800 in Fig. 49. The devices were selected to have a similar I_{dss} for fair comparison. The results are all quite similar. Device 3-1605 shows the earliest pinch-off characteristics as there is no appreciable current at a gate bias of -0.2 volts whereas the other devices still show significant drain current at this gate bias level. This result is consistent with expectations based on channel depth. The narrowest channel is pinched-off first. The harder saturation expected with the narrower channel, and observed in the two-dimensional simulations is not apparent in the results. This may be because the predicted harder saturation was slight (Fig. 26) and the prediction was for a four-fold reduction in channel depth. The reduction in channel depth between device 3-1603 and 3-1605 is only 36%. Comparison to device 3-1800 is

not conclusive because of the two-layer nature of the channel: 400 Å $In_{.6}Ga_{.4}As$ and 400 Å of lattice-matched InGaAs.

The 94 GHz noise performance of the three devices is shown in Table II, and the gain as

TABLE II

Wafer No.	V_{ds}	V_{gs}	I_{ds} (ma)	NF(db)	Gain	F_t (GHz)
3-1603	0.75	0.005	7.0	1.8	5.8	150
3-1605	0.75	0.06	8.0	1.5	5.6	150
3-1800	0.75	-0.05	7.0	2.1	6.1	145

a function of frequency is shown in Figs. 50 to 52. We note that the noise level for wafer 3-1605 is very close to the lowest noise yet obtained for such a device and wafer 3-1603 had a device with f_{max} of over 480 GHz, the highest value for f_{max} yet reported!

V.6. COMPARISON OF PREDICTION AND EXPERIMENT

In view of the data obtained for the preliminary wafers it was deemed appropriate to test the predictions capability of our two-dimensional quantum hydrodynamics model against the data. For these purposes, wafer 3-1605 was chosen. The results of the simulation are presented in Figs. 53 and 54. The DC I-V characteristics are shown in Fig. 53. The agreement between simulation and measurement at gate bias levels of 0.4 and 0.2 volts is excellent. However, at V_{gs} = 0.0 volts we

see a significant reduction in transconductance. The variation in transconductance, capacitance and cutoff frequency given by the simulations are shown in Fig. 54 for V_{ds} = 1.0 volts. Obviously, the actual device has less variation in g_m. We also note that the cut-off frequency is higher than that measured by about 20%. In view of the good agreement between predicted and measured I-V characteristics above V_{gs} = 0.2 volts, it is apparent that the device capacitance is under-predicted.

From our parametric investigation we know that the device capacitance can be increased by a number of factors including increasing the depth of the gate recess, reducing the spacer layer thickness or increasing the planar layer doping. We also note that the predicted I-V curve shows reduced transconductance at lower gate bias levels compared to that which was measured. These factors, taken together, suggest that the charge sheet density in the channel, under the gate, is too low in the simulations. This can be the result of either too low a doping of the planar layer, or too great a barrier height at the Schottky contact. We also recognize that, as indicated by Eqs. (3) and (31), an increase in capacitance through an increase in charge sheet density will result in increased transconductance unless the saturation velocity is reduced. Since the predicted values of cutoff frequency are nominally 20% too high, a 20% increase in capacitance required while maintaining the nominal levels of transconductance and drain current. Elimination of V_s between Eqs. (30) and (31) tells us this can be accomplished through a 20% increase in sheet density and a corresponding 20% reduction in saturation velocity. Eq. (32) shows the reduction in f_t requires a similar reduction in V_s as well. From our two-dimensional simulation results, shown in Figs. 17 and 21, we also note that an increase in sheet density will yield a transconductance and capacitance which are weaker functions of gate bias, another characteristic which would bring the predicted result into better agreement with the data. We therefore conclude that either the barrier height or planar layer

doping are different between the real and simulated structures. Another factor, which may influence the transconductance at low bias levels, is the treatment of the contacts. Recall we have eliminated the barriers under the source and drain contacts. This may remove some physical aspects of tunneling current at the contacts which may influence the current at low bias levels. We were, unfortunately, unable to confirm this under the present research effort through additional simulation, but it is clear that refinement of these quantities would bring the simulated results into better agreement with the measurements.

V.7. OPTIMIZATION OF THE HEMT DESIGN

Based on the results of the preliminary structures and the parametric investigation conducted numerically, a consensus was reached that increasing the sheet density in the channel would be beneficial to the device performance. SRA also suggested that the cap layer doping be increased. These changes were expected to further improve the noise performance of the device by lowering the source resistance and increasing the cutoff frequency. We recall that Eq. (24) gives the minimum noise figure as a function of source resistance, capacitance, transconductance and channel resistance. Increasing the doping of the cap layer was recommended to reduce the source resistance. The increase in sheet charge would contribute to reduced source resistance, and also reduced input or channel resistance, thus possibly increasing noise. However, our parametric study revealed that increasing the channel charge sheet density, either by increased planar layer doping or by a reduction in the spacer layer thickness, should increase the cutoff frequency. This will reduce

noise, in accordance with Eq. (24), since a higher value of cutoff frequency represents a lower value for the ratio to C_g/g_m.

The technique decided upon to increase the charge sheet density in the channel was a reduction in the thickness of the spacer layer from 45 Å to 30 Å. The proposed wafer structure, referred to as wafer no. 3-2259, is shown in Fig. 55. The cap layer was doped to $2x10^{18}/cm^3$. The depth of the channel was 275 Å with an additional 125 Å layer of lattice matched InGaAs yielding a 400 Å channel. This structure is similar to that of wafer no. 3-1603 with a reduction in the spacer layer and the additional 125 Å InGaAs layer. To verify that the reduced spacer layer would yield an increased charge sheet density and improved performance, a second wafer structure was proposed as a control. This wafer, referred to as wafer no. 3-2086, is shown in Fig. 56. The structure is similar to that of wafer no. 3-2259 with the exception of the spacer layer thickness which is 42 Å. The mole fraction of In in the 400 Å deep channel has also been reduced to allow a stable structure.

Prior to processing of the wafers, SRA applied its one-dimensional workstation software to predict the charge distribution in the new structures. A comparison between the optimized and control wafers is shown in Fig. 57. The total concentration of dopants is the same in both structures. The linear plot of the charge distribution clearly shows greater accumulation of charge in the channel and less in the cap layer for the optimized structure (wafer no. 2259). The log scale plot additionally shows greater depletion of the PD layer and less charge overall in the isolation layer. The reduced spacer layer has had the desired effect. The predicted result yielded a 15% *increase* in charge in the channel of the optimized structure as compared to the control. This represents a similar *reduction* in the cap layer since the total charge in both structures is equal. The

reduction of the charge in the cap layer should also be beneficial since it will reduce parasitic capacitance.

Measurement of the two wafers confirmed the predicted results. The optimized structure was found to have 17% greater charge sheet density in the channel as compared to the control structure, in good agreement with the prediction.

V.8. PERFORMANCE OF THE OPTIMIZED STRUCTURE

InP HEMTs were processed from the optimized and control wafers. A total of five wafer pieces were processed: 3 real ones and 2 dummies for gate process tests. The wafers were fabricated using the same process as that for the preliminary lot. The device layout is also the same, a 0.1 μm by 30 μm T-gate.

During the wafer process it was noticed that the mesa isolation voltages of these wafers were about 20% to 40% lower than those of the previously processed lot. This was due to a higher impurity level in the InP substrate. These substrates were supplied by a different vendor than those of the preliminary lot. Based on test results it was found that the higher impurity levels in the substrate had virtually no effect on the device DC performance. It does, however, introduce extra parasitic capacitances and could contribute to a slight degradation in the noise figure and RF gain, particularly at frequencies approaching 94 GHz.

The device process was carried out very smoothly. Excellent DC characteristics were obtained, as shown for device 3-2259-5 in Fig. 58 and device 3-2086-1 in Fig. 59. Table III summarizes the DC performance of these devices. Room temperature extrinsic transconductance

TABLE III

Wafer No.	Transconductance (ms/mm)	Source Resistance (Ω-mm)
3-2259-3	1100	0.13
3-2259-5	1330	0.13
3-2086-1	820	0.22

as high as 1330 ms/ms and excellent pinch-off characteristics were obtained from wafer 3-2259. The device source resistance was a record low 0.13 Ω-mm, a 24% reduction over the best of the preliminary structures. *These represent the best DC characteristics yet achieved at the Martin Marietta Laboratory. The results clearly demonstrate the value of the simulation tools developed as part of this effort in aiding in the design of an optimized structure.*

The sample devices were also probed to obtain RF characteristics and noise figures. All of the devices had cut-off frequencies in the 150 GHz range, similar to the preliminary structures. We had anticipated improved values. However, as previously noted, the high level of impurities in the InP substrate for the new devices resulted in additional parasitic capacitances. In light of this, it is reasonable to expect that given substrates of similar quality, superior performance would be obtained from the optimized device structure. Table IV summarizes the RF performance of these devices. The noise figures are very good, in the range of 2dB at 94 GHz, as is the gain of devices from wafer 3-2259. These results are superior to those of wafer 3-2086 verifying the conclusions from the simulations and analysis that the higher charge sheet density should be beneficial to the

HEMT noise and speed performance. Again, with a better insulated substrate, we would expect even lower noise and high gain from these (3-2259) wafers.

TABLE IV

Wafer No.	V_{ds}	V_{gs}	I_{ds} (ma)	NF (dB)	Gain (dB)
2086-1	0.9	-0.07	5.0	2.4	4.5
2259-3	0.9	-0.08	6.0	2.1	5.0
2259-5	0.9	0.09	5.6	2.1	5.6

VI. SUMMARY

A combined theoretical and experimental program was undertaken in an effort to design and fabricate InP-based PHEMTs with 0.1 μm gate suitable for low noise, high speed application. The theoretical aspects of the investigation were performed by Scientific Research Associates, Inc. and involved the formulation of one- and two-dimensional quantum corrected hydrodynamics models and numerical solution algorithms. A workstation interface was developed for the one-dimensional simulation tool which allowed easy and rapid evaluation of proposed HEMT wafer structure. The more complex two-dimensional simulation tool allowed detailed predictions of the transport within the HEMT structures to be made. Both the one- and two-dimensional models were used in

accessing device performance and in conducting a parametric study of design factors influencing the performance of the basic 0.1 μm HEMT structure considered in this study.

The experimental aspect of the study was performed by Martin Marietta Electronics Laboratory. Various wafer and HEMT structures were fabricated and tested for DC and RF performance in the 94 GHz range. On the basis of the measured performance of several preliminary devices and the results of the theoretical predictions, device modifications were proposed in an effort to optimize the high frequency and noise performance. A new device was fabricated and tested, and was found to have excellent DC and high frequency performance.

The results of the present study demonstrate that advanced simulation tools can be used as an integral part of the design and optimization procedure for state-of-the-art device structures. The HEMT structures fabricated under the present effort have obtained some of the highest performance figures yet reported for 0.1 μm gate length InP HEMTs operating in the 94 GHz range. Noise figures as low as 1.5 dB were obtained at 94 GHz with f_{max} of over 480 GHz for specific devices.

VII. ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of Dr. P.C. Chao, of the Martin Marietta Electronics Laboratory, under whose direction the experimental work was performed.

VIII. PUBLICATIONS

The following publications were a result, either in part or in whole, of work performed under this contract.

J.P. Kreskovsky and H.L. Grubin, "Electron Transport Using the Quantum Corrected Hydrodynamics Equations," VLSI Design, to appear, 1994.

J.P. Kreskovsky and H.L. Grubin, "Transport in Two-Dimensional Quantum Well HEMTs," in Proceedings of the 1994 International Workshop on Computational Electronics, to appear, 1994.

IX. PARTICIPATING PERSONNEL

The following scientific personnel participated in this project:

Scientific Research Associates, Inc.

Dr. Harold L. Grubin

Mr. John P. Kreskovsky

Martin Marietta, Inc.

Dr. P.C. Chao

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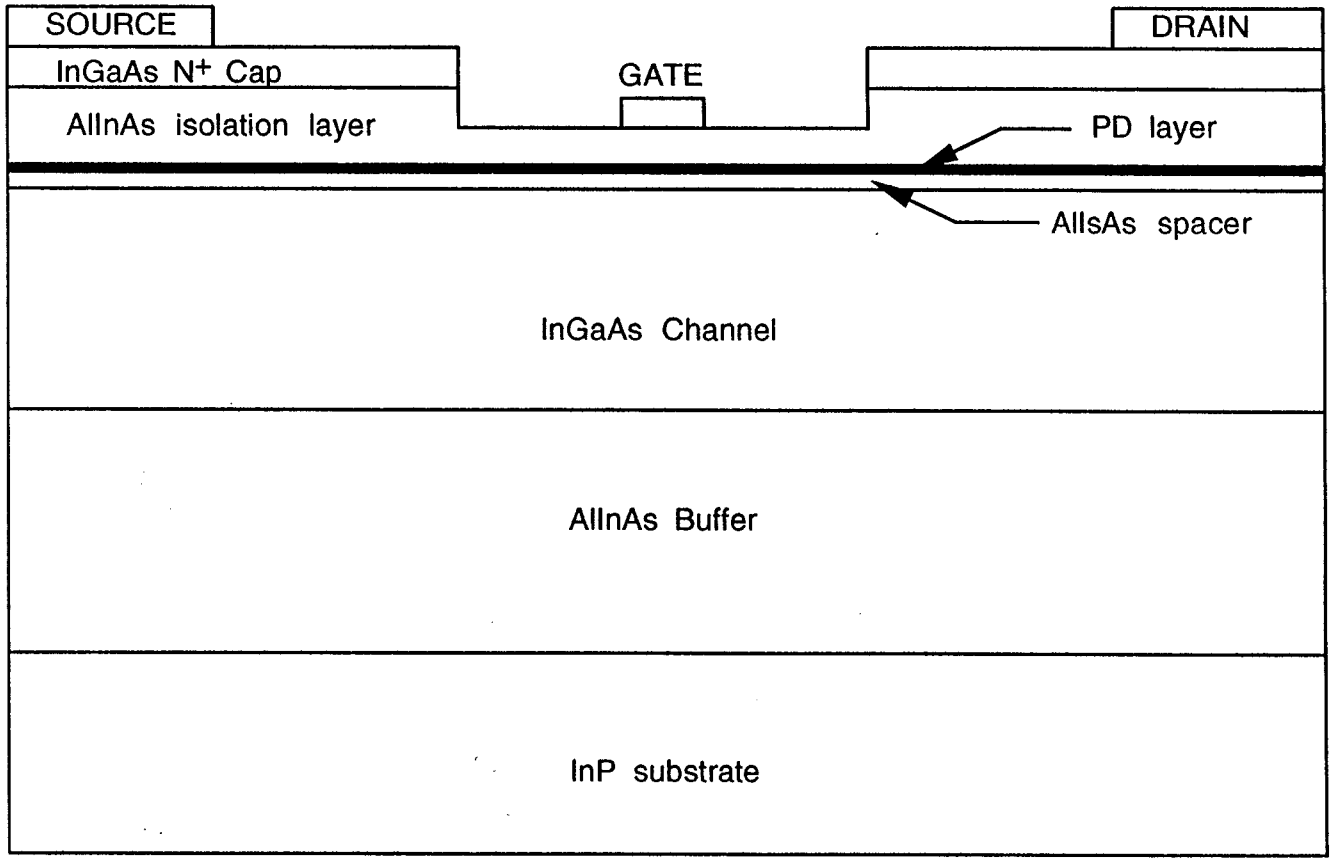


Figure 1. Schematic representation of InP HEMT.

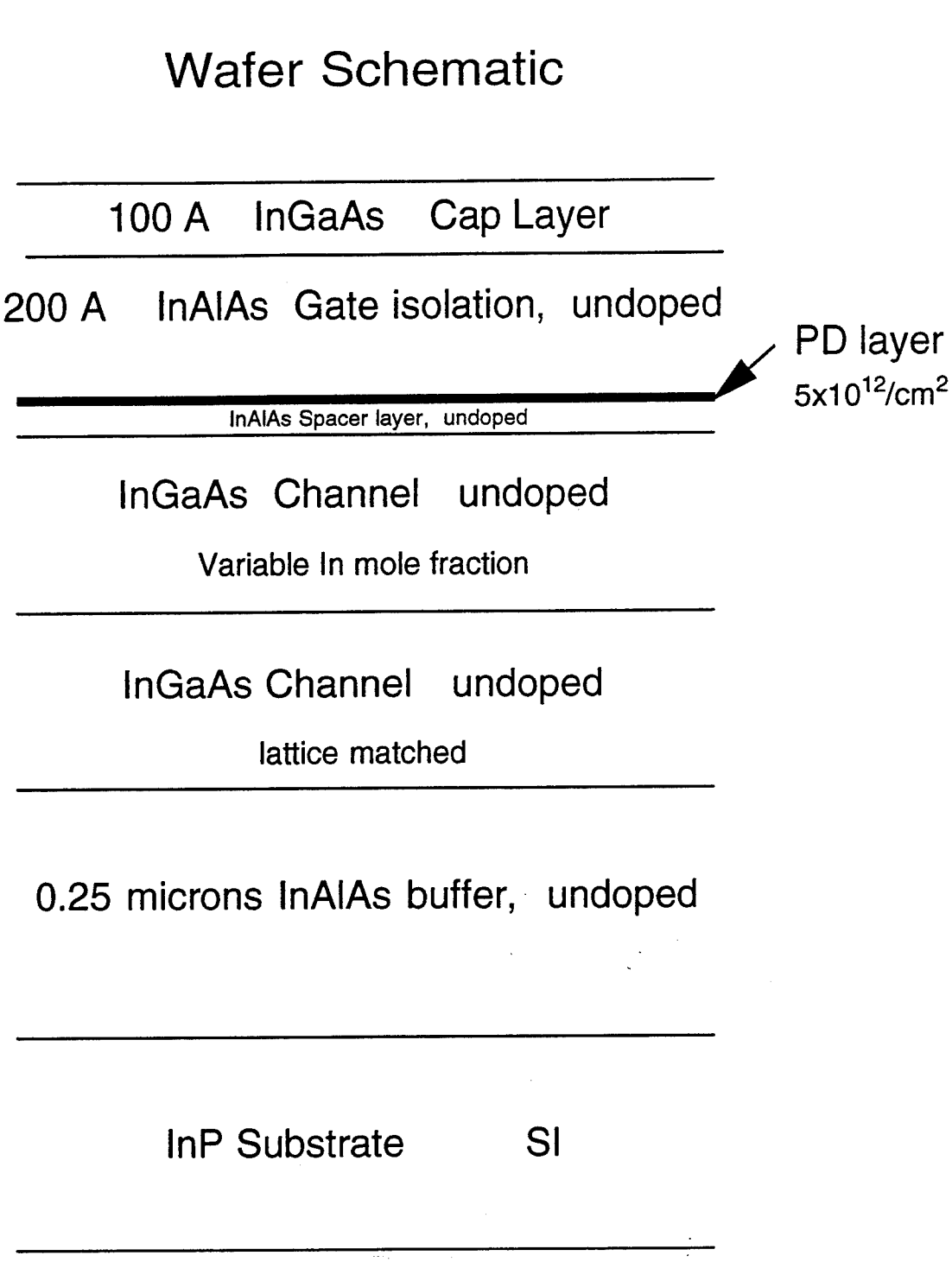


Figure 2. Schematic of HEMT wafer structure.

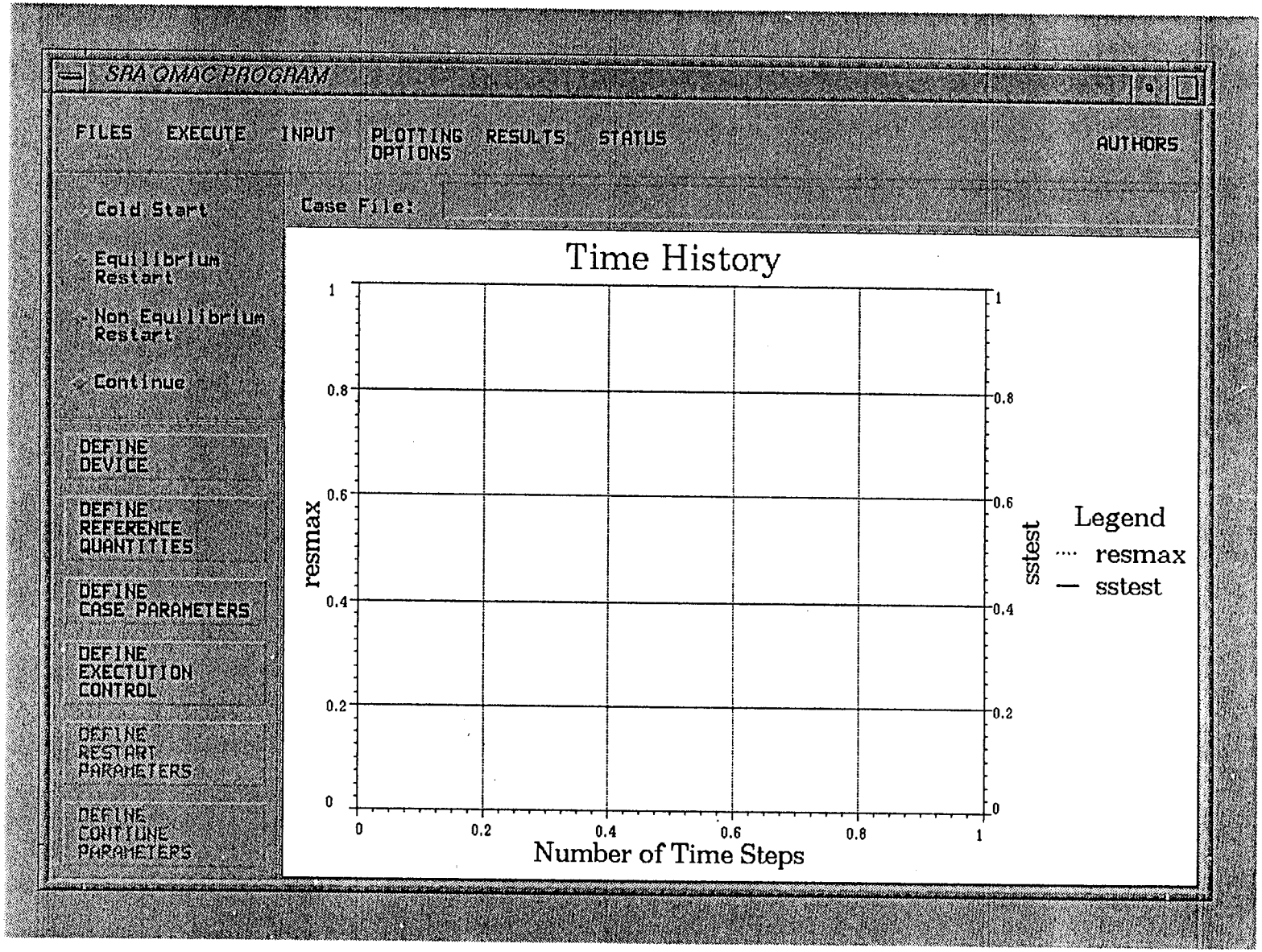


Figure 3. One-dimensional quantum-hydrodynamics workstation code control window.

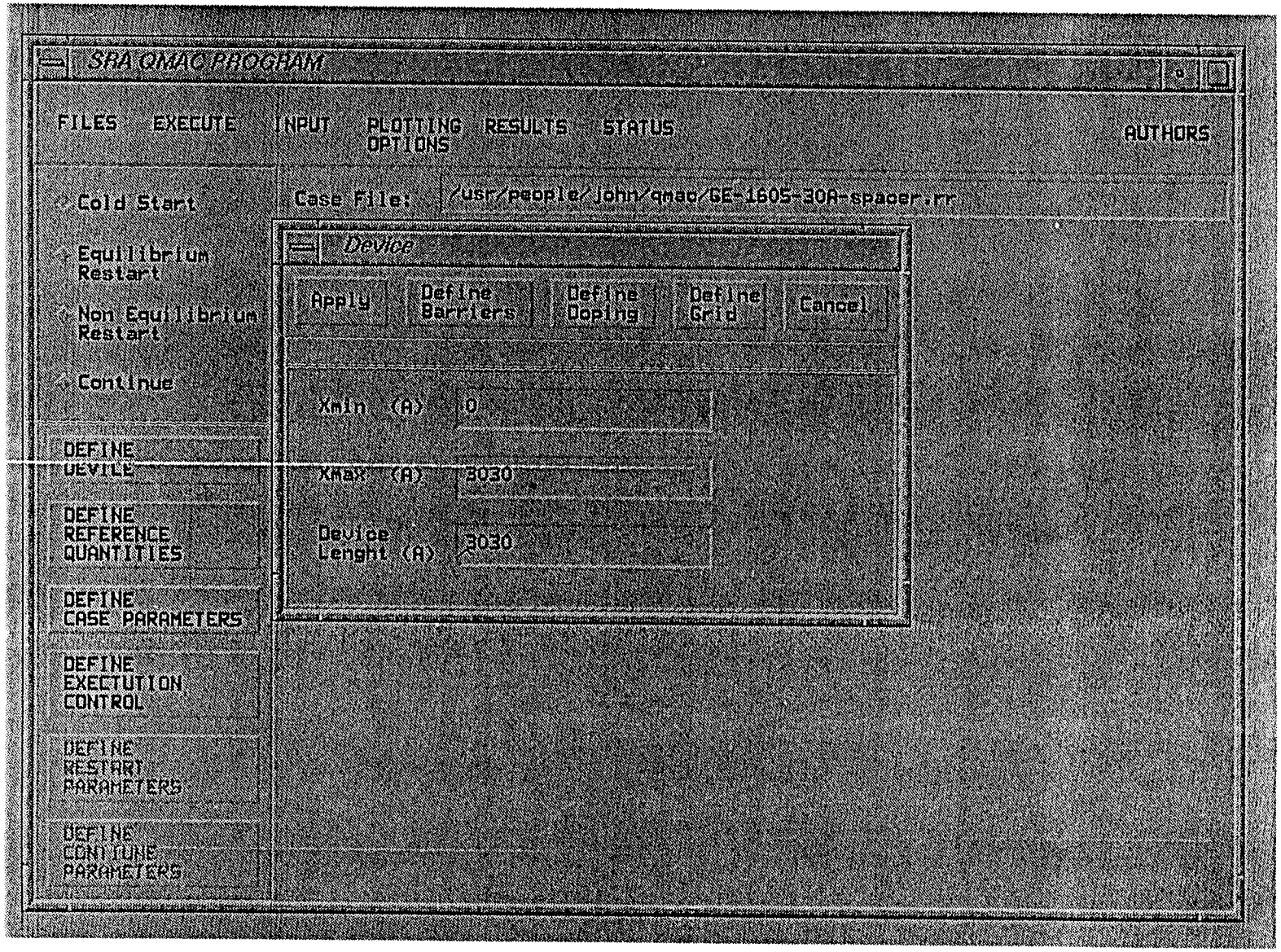


Figure 4. Workstation control and device definition windows.

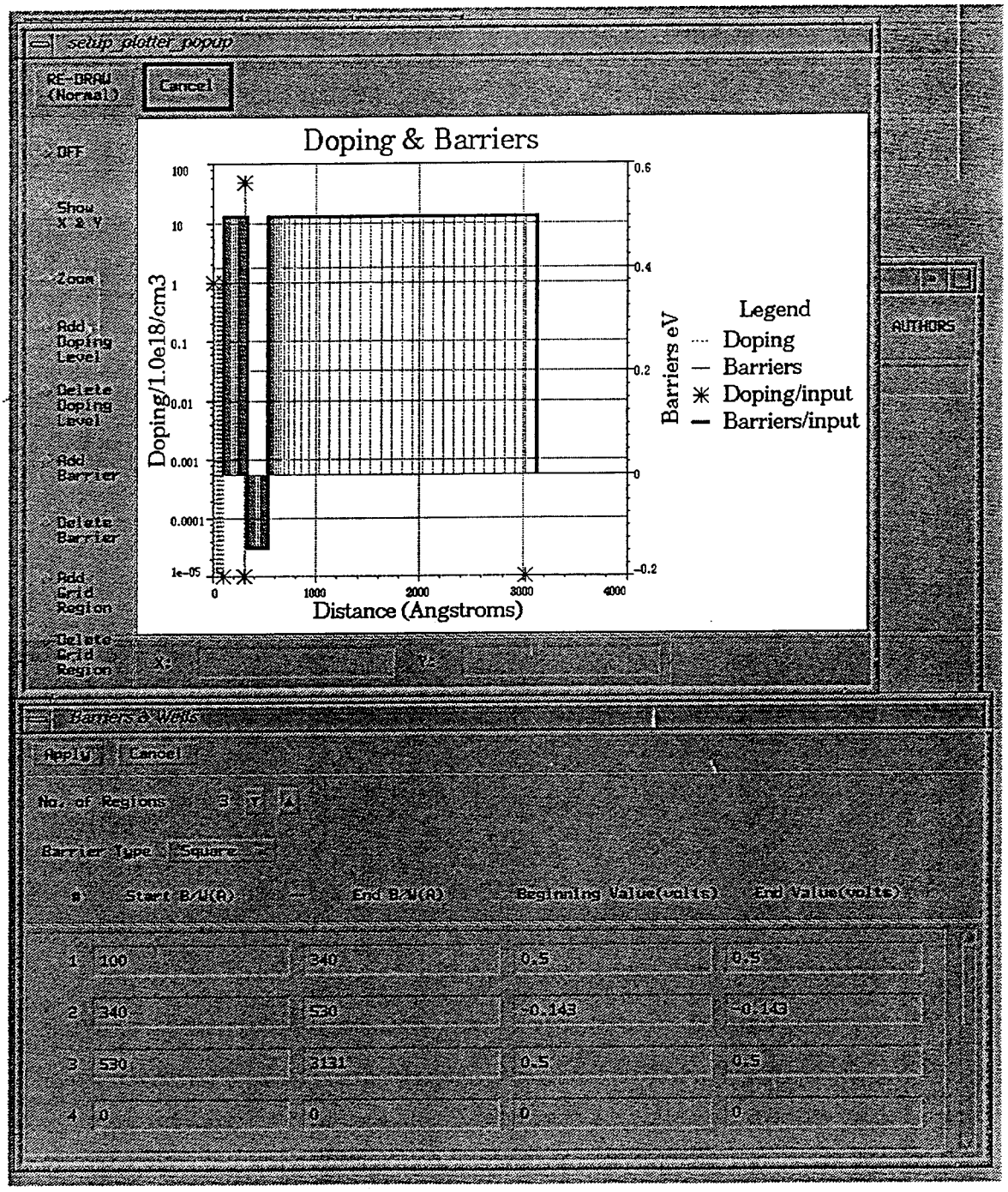


Figure 5. Workstation barriers and doping setup windows.

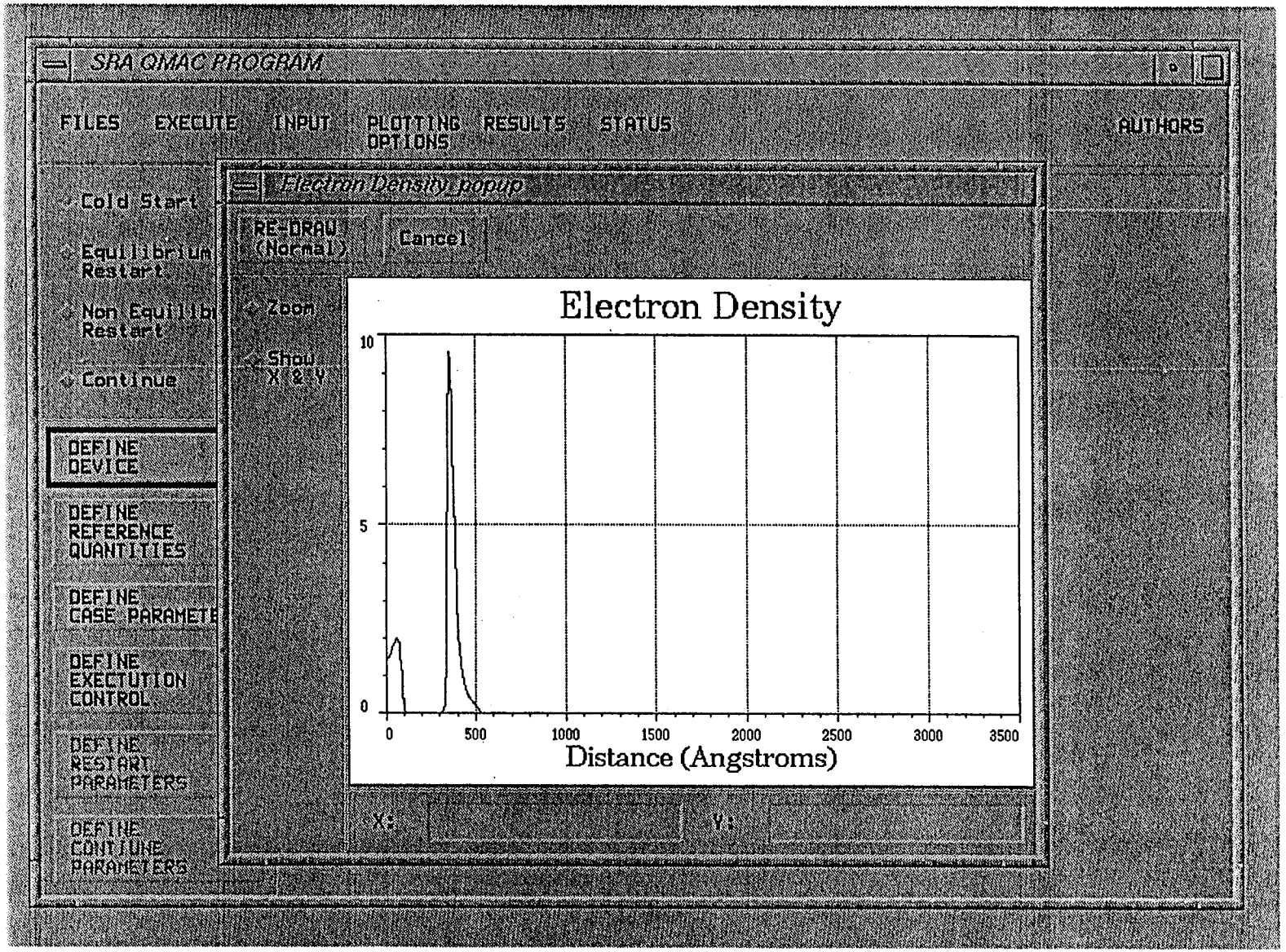


Figure 6. Typical workstation display of graphical results.

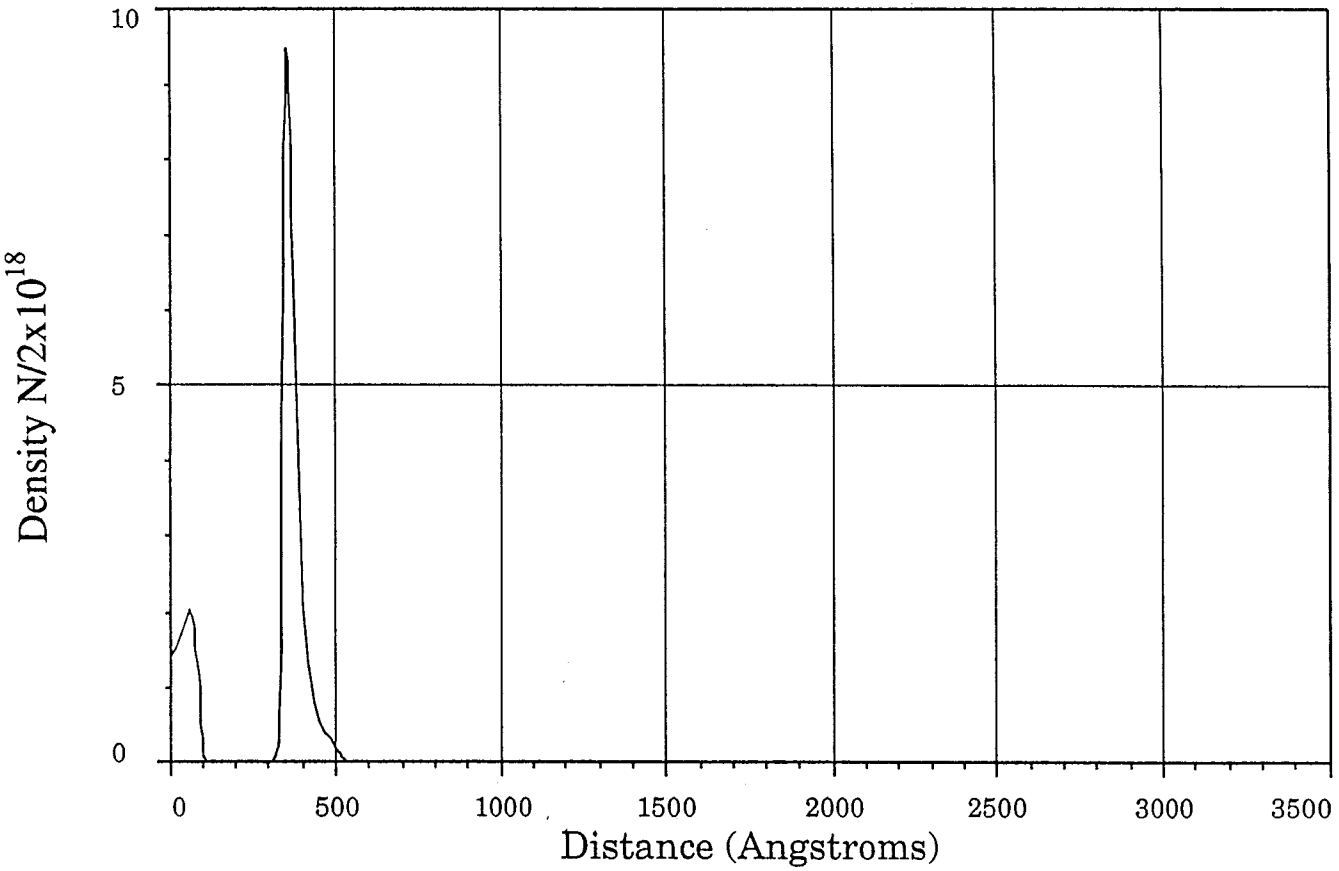
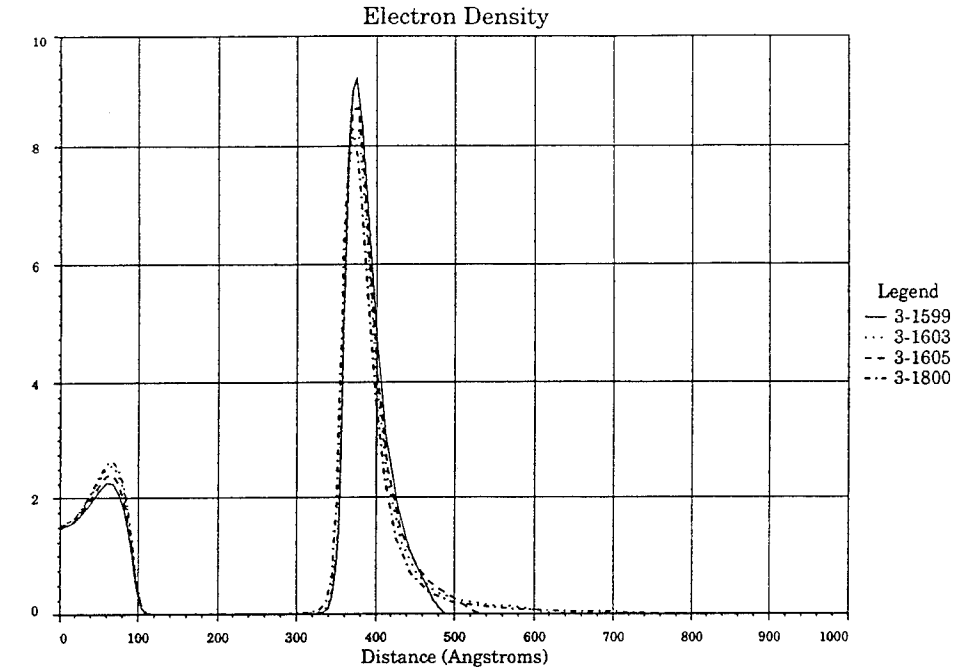


Figure 7. Workstation generated laser printer report figure.



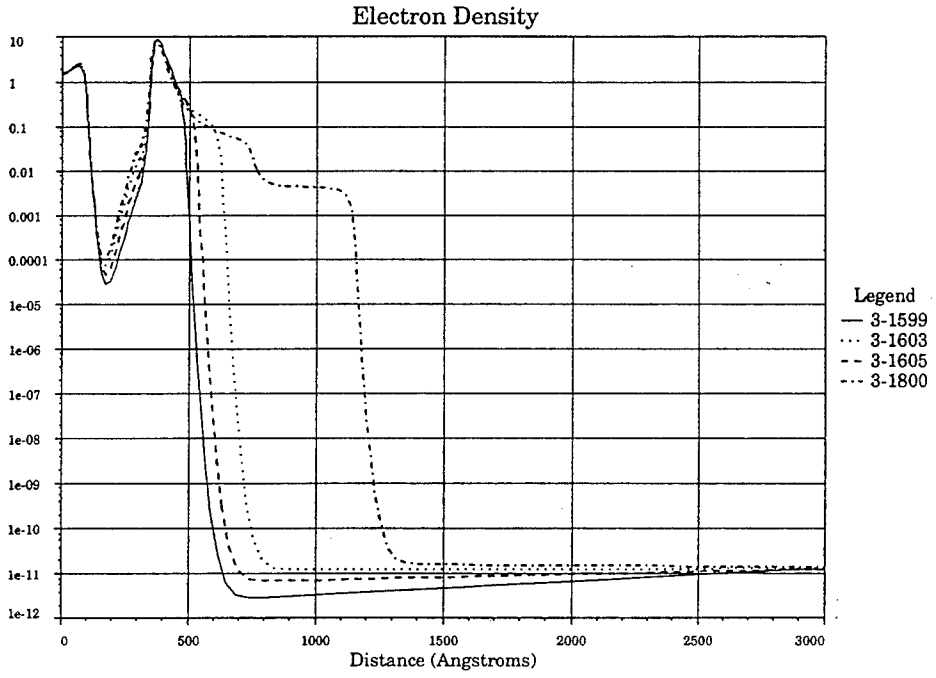


Figure 8. Linear and logarithmic comparison of the charge distribution in the preliminary wafer structures.

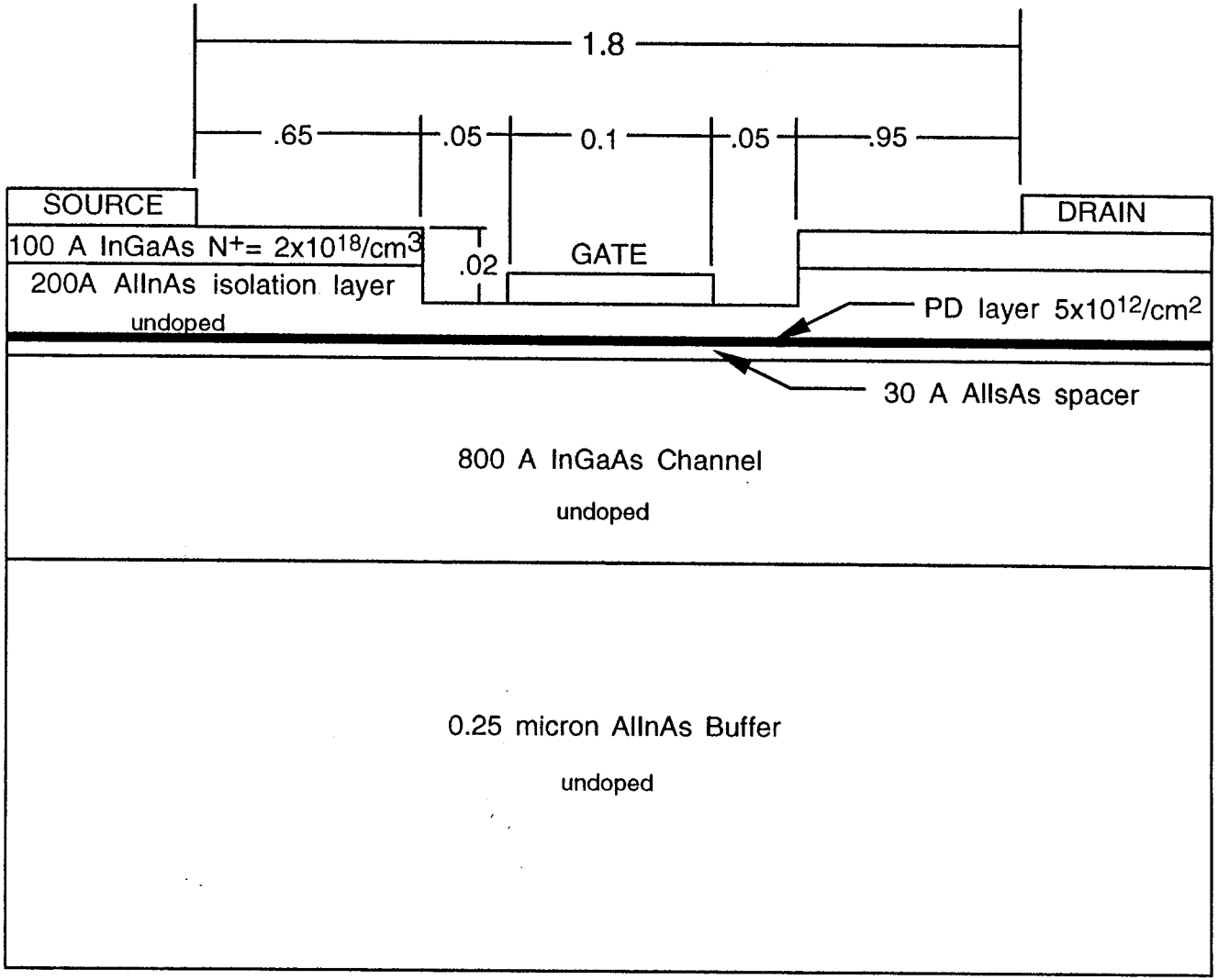


Figure 9. Details of reference device structure for parametric study.

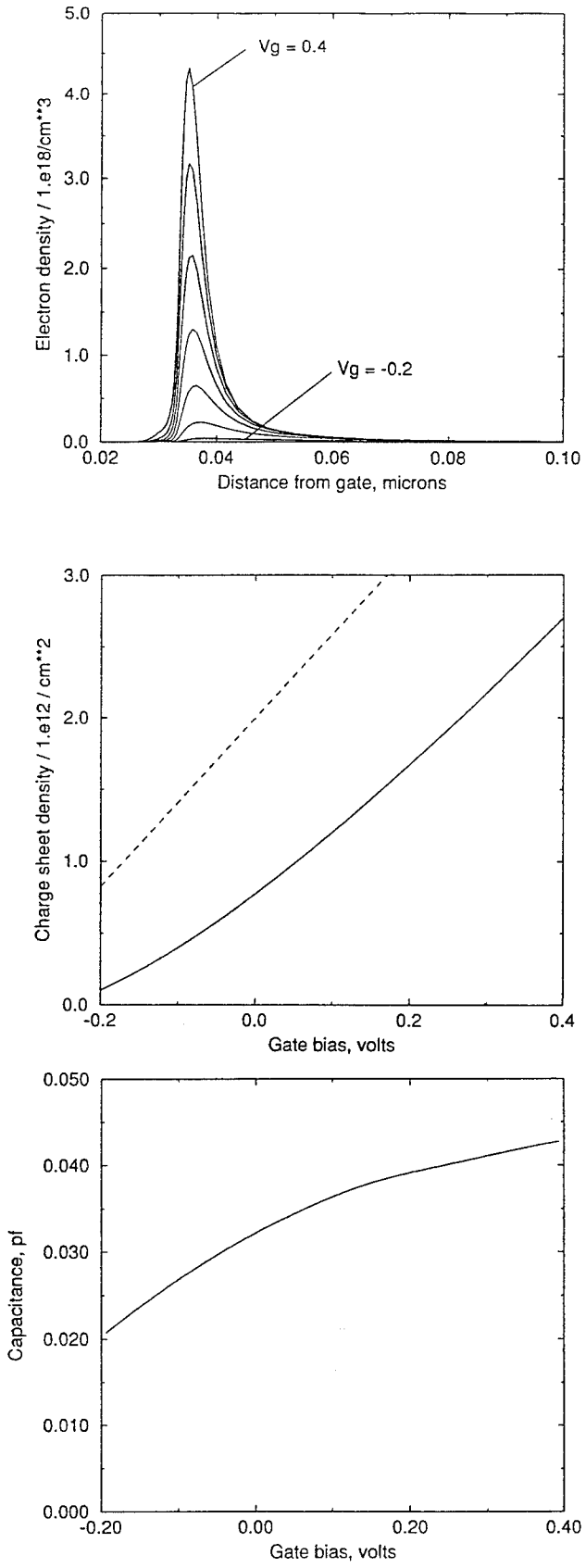
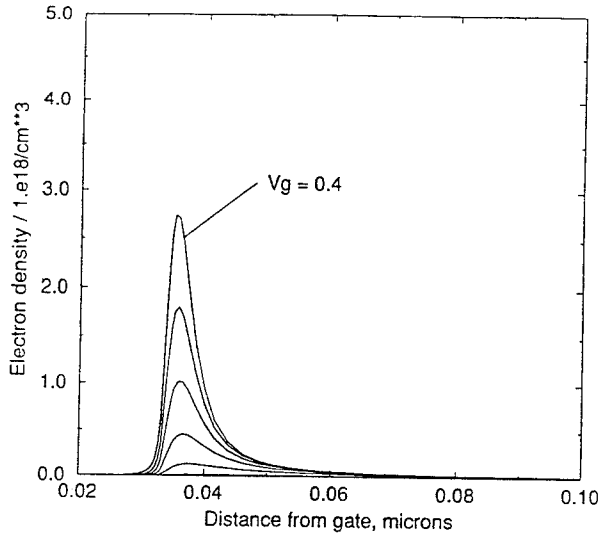
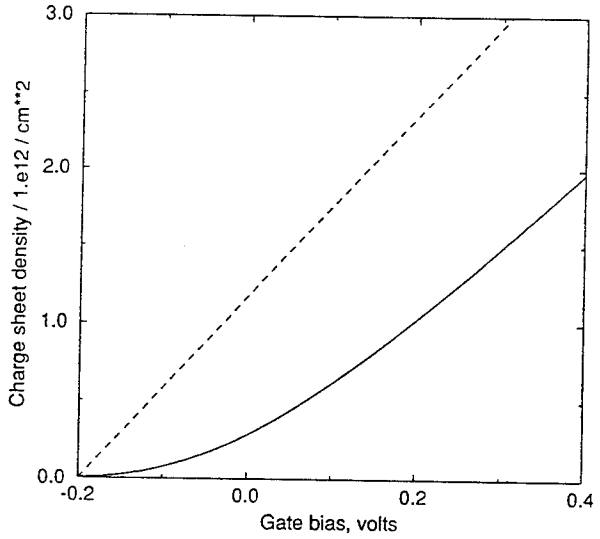


Figure 10. Electron distribution, charge sheet density and capacitance as a function of gate bias as predicted from the one-dimensional code for the reference device.





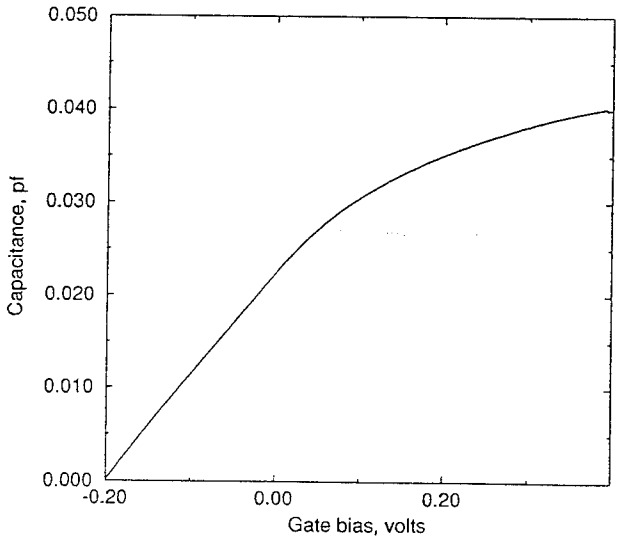
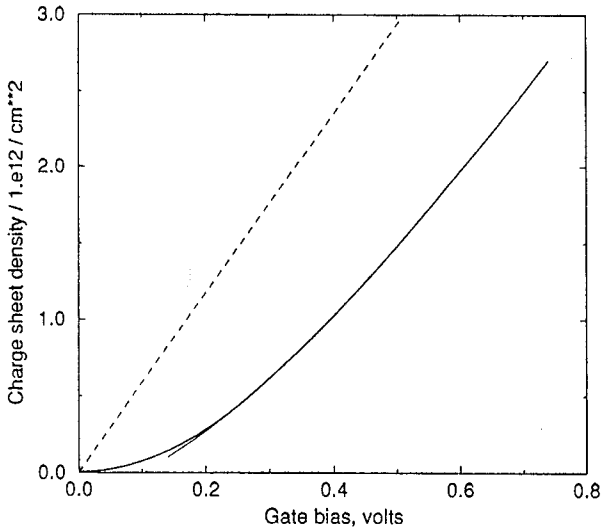


Figure 11. Similar to Figure 10 but for a 20% reduction in planar layer doping.



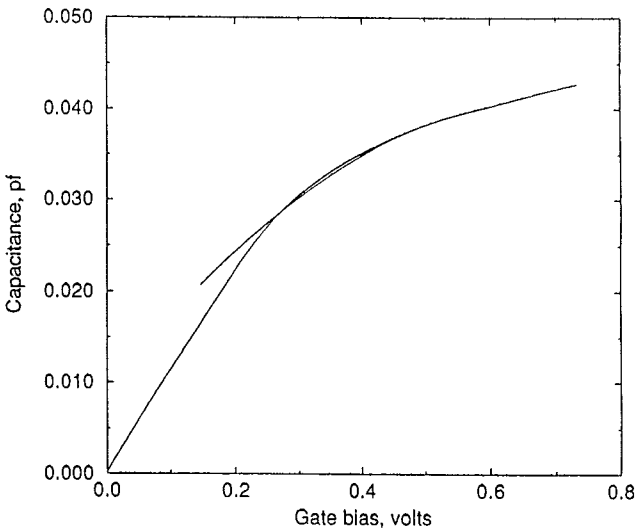
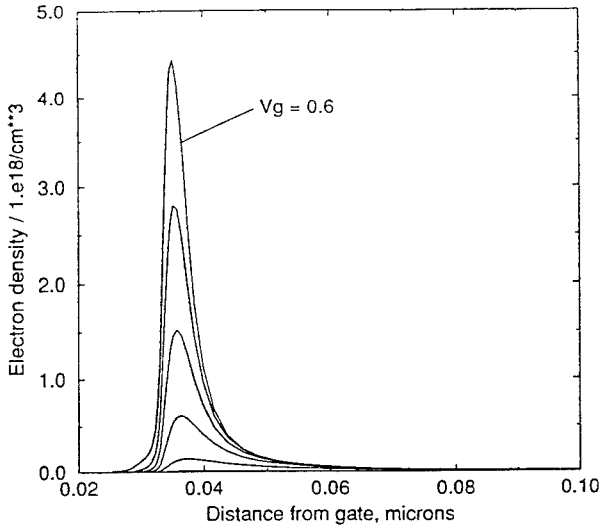
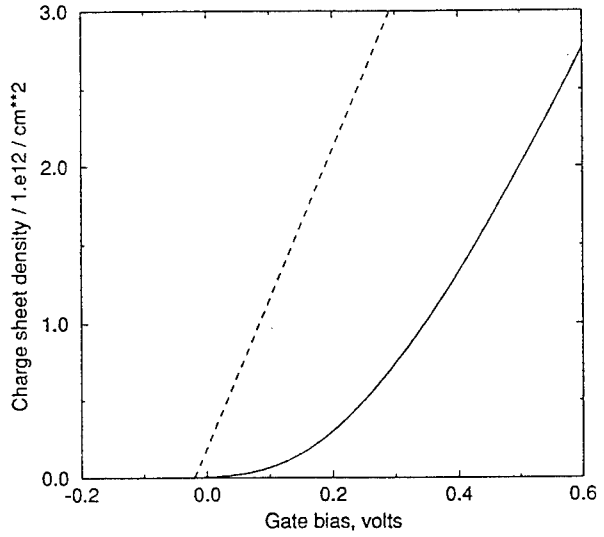


Figure 12. Charge density and capacitance for reference device and 20% reduction in planar layer doping shifted for threshold voltage.





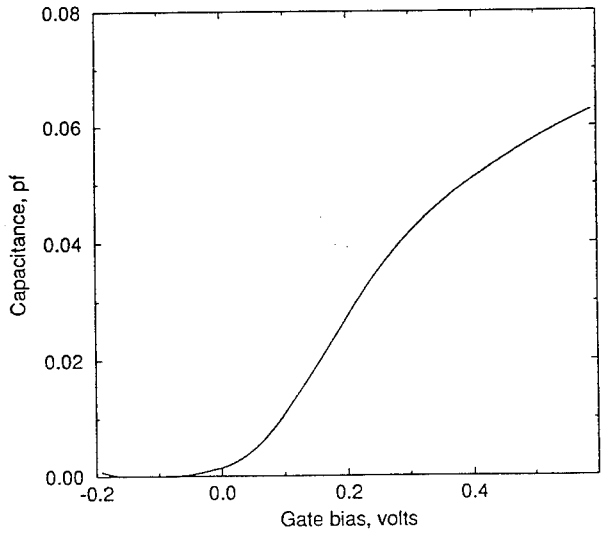


Figure 13. Similar to Figure 10 but for increased gate recess.

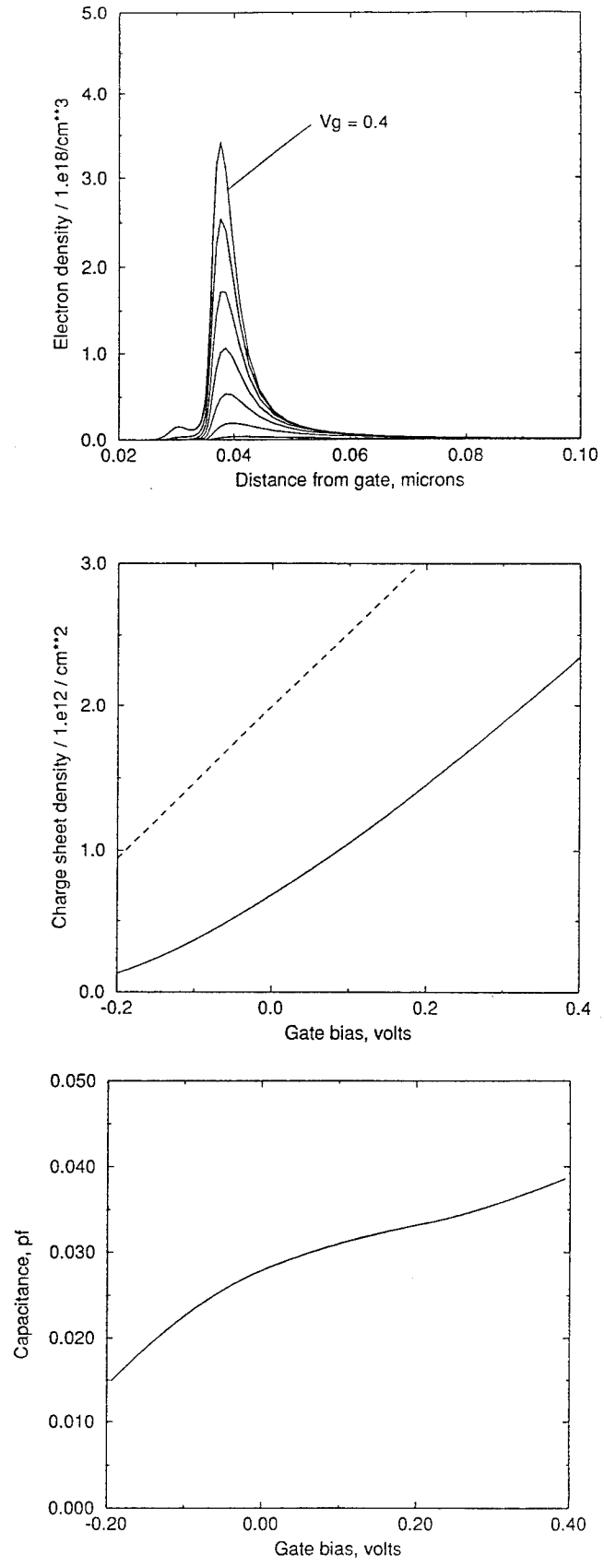
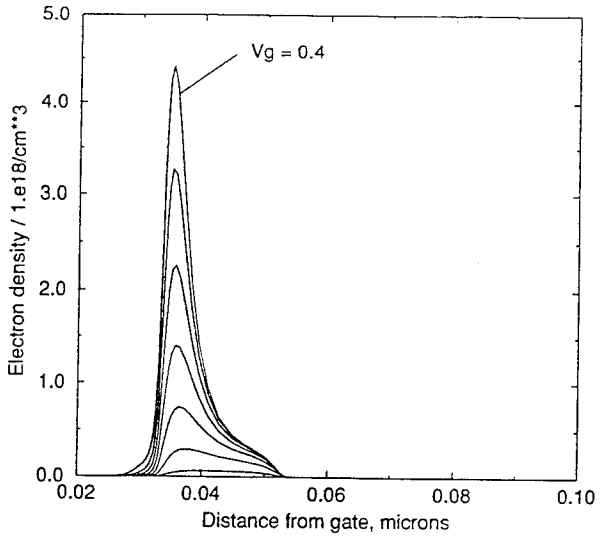
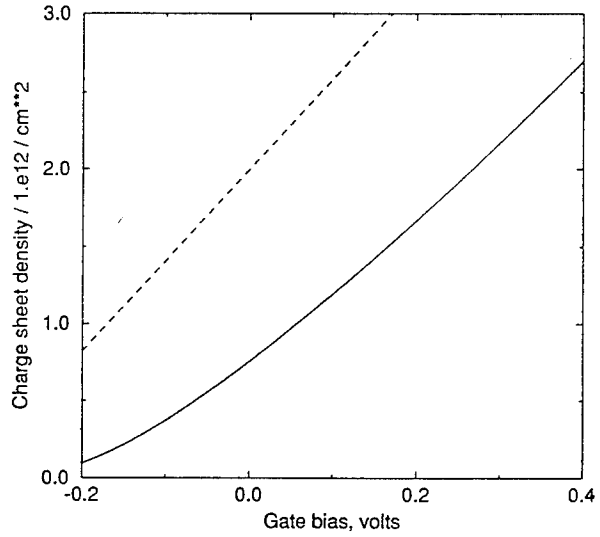


Figure 14. Similar to Figure 10 but for increased spacer layer thickness.





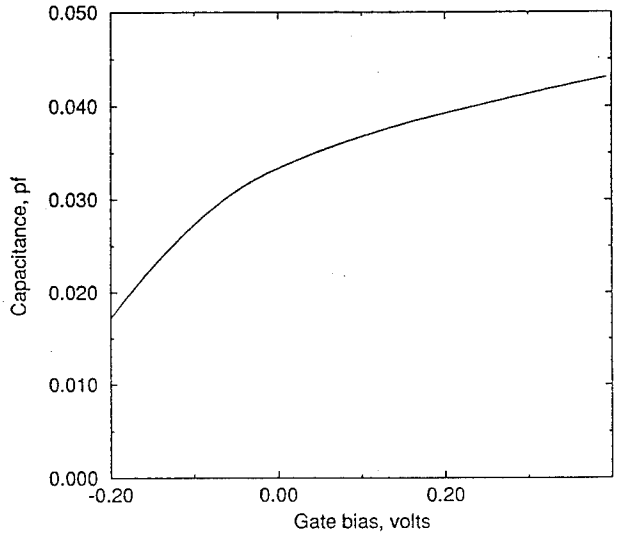


Figure 15. Similar to Figure 10 but for reduced channel depth.

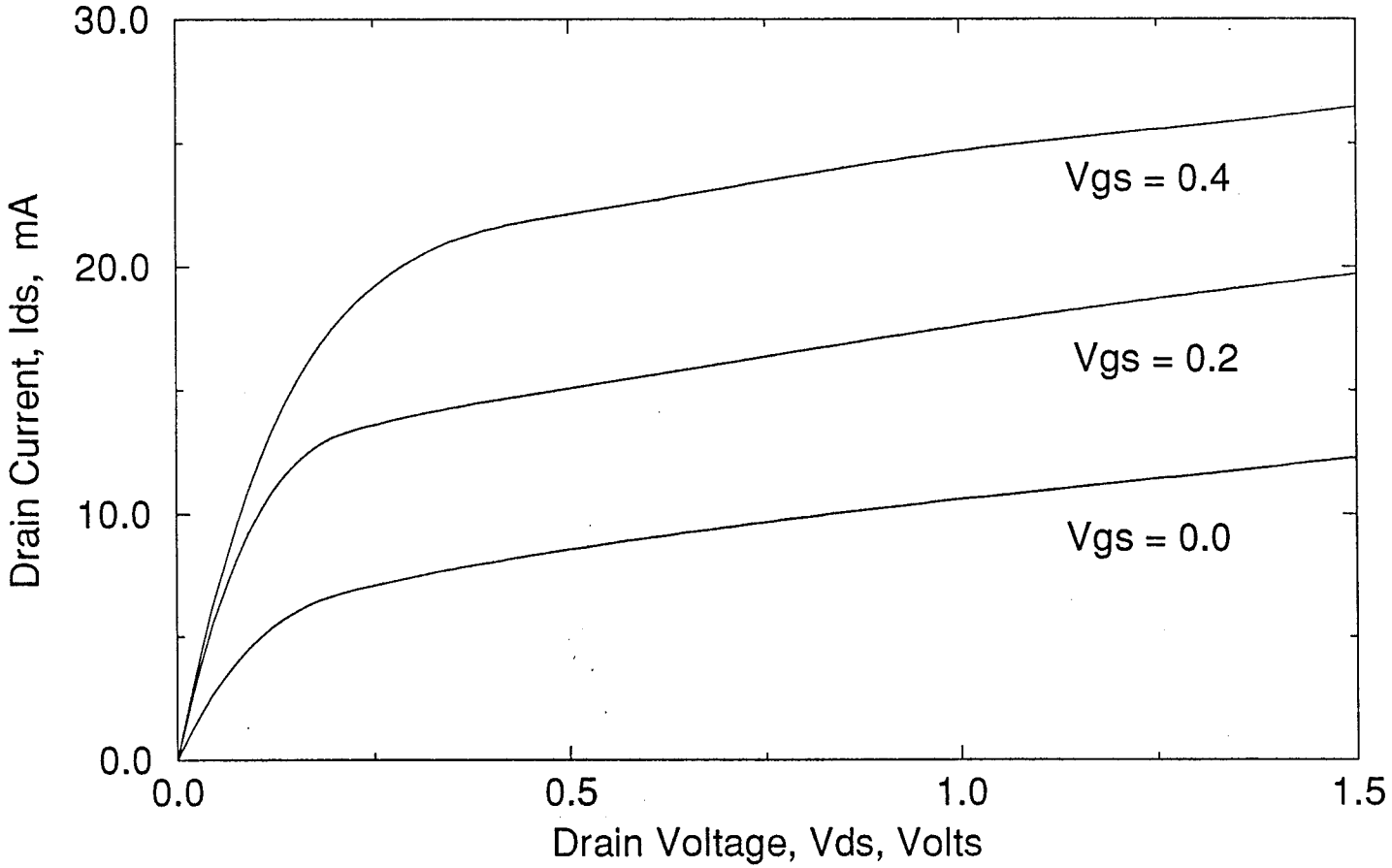
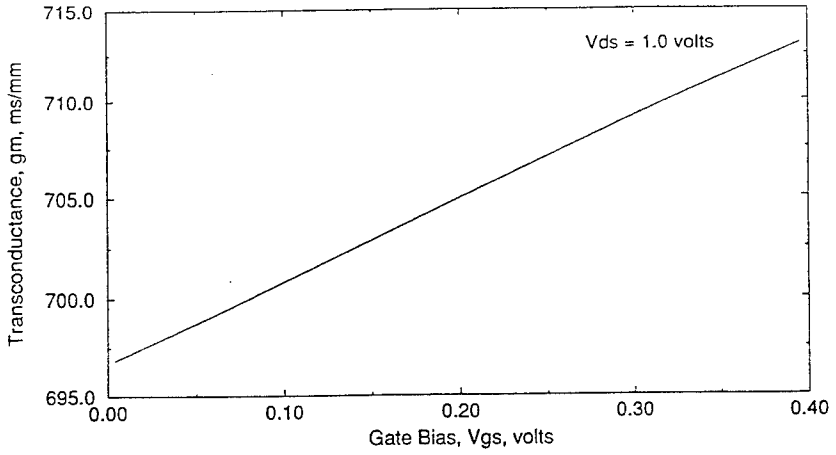
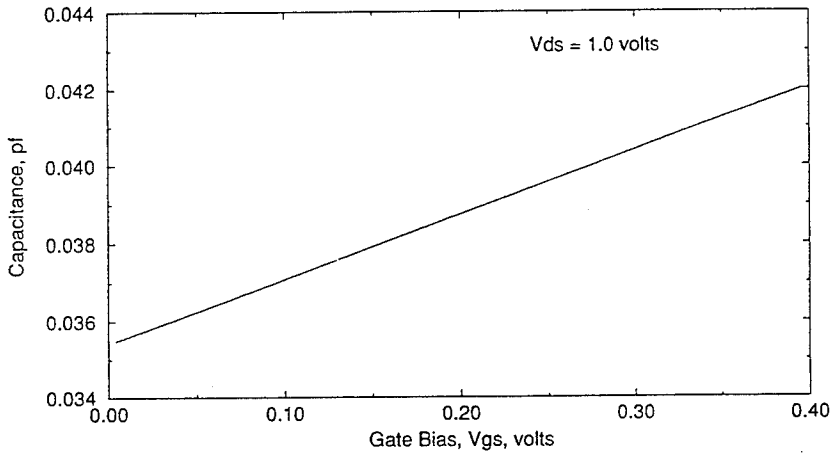


Figure 16. Current-voltage characteristics from two-dimensional simulation code for the reference structure.





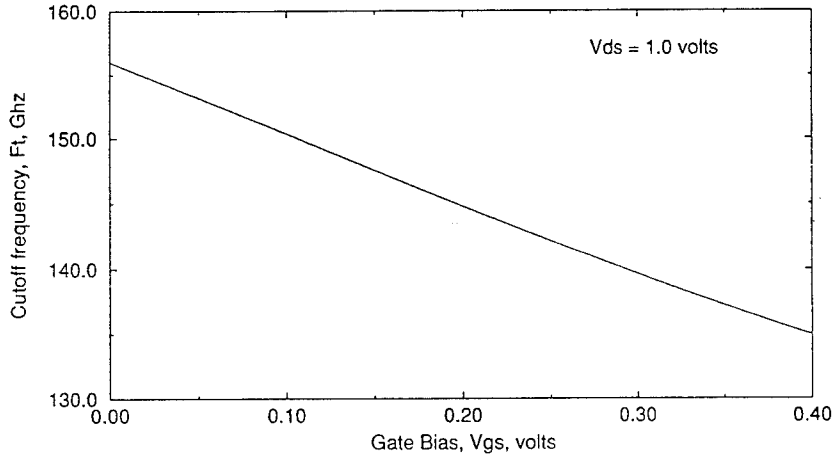


Figure 17. Predicted transconductance, capacitance and cut-off frequency for the reference structure as obtained from the two-dimensional simulation code.

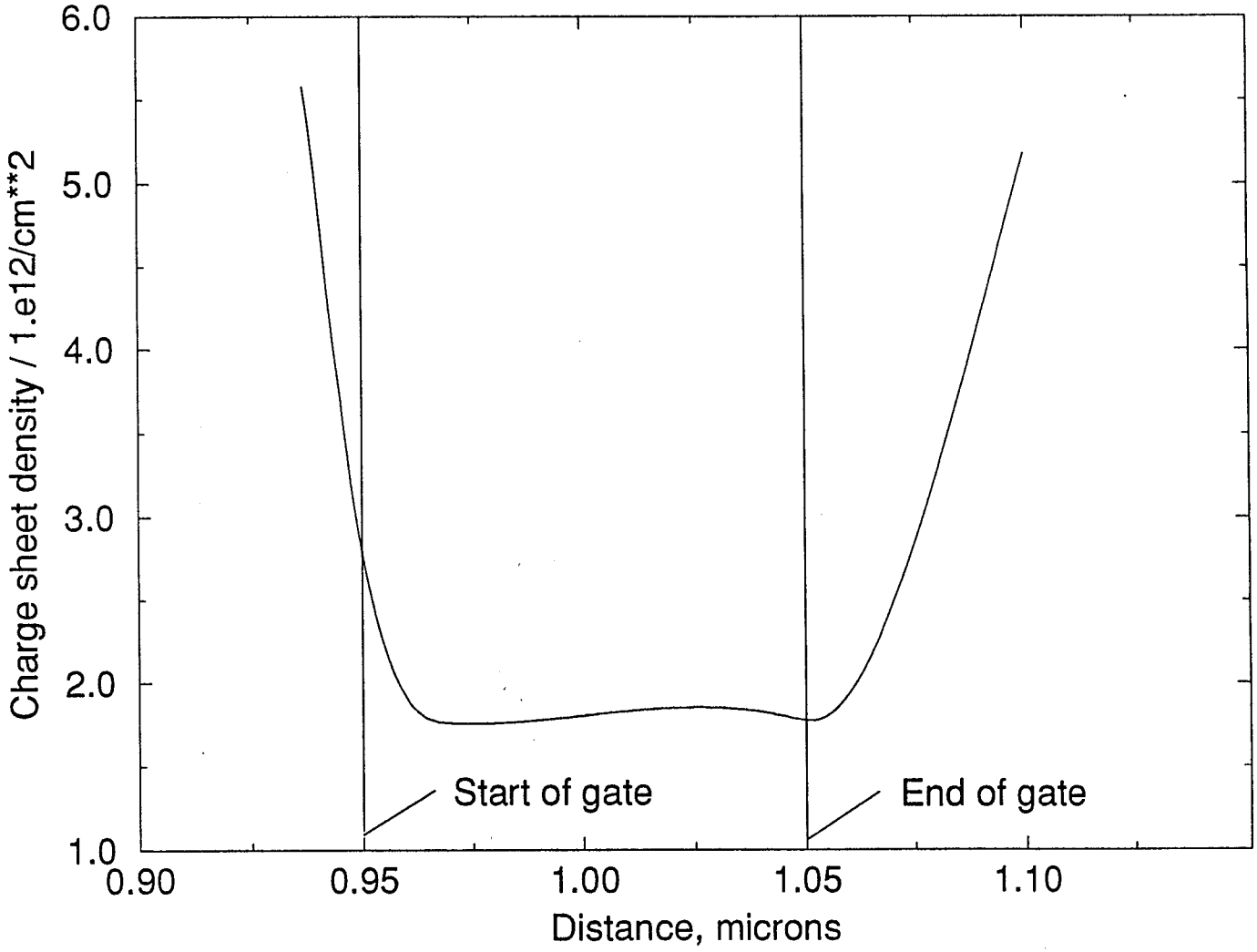


Figure 18. Variation of sheet charge density under the gate predicted from the two-dimensional simulation code for the reference structure.

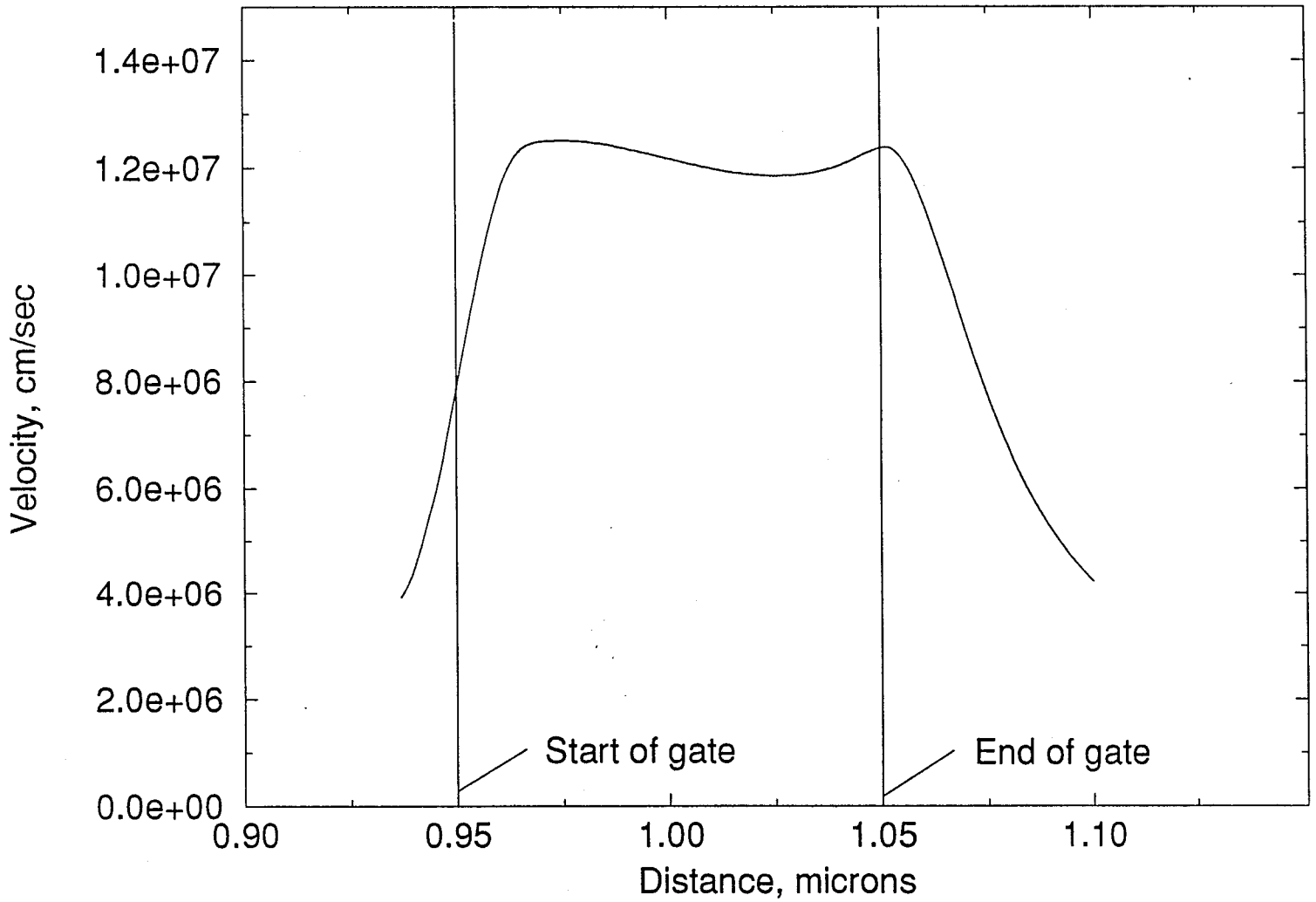


Figure 19. Average velocity across the channel as a function of distance along the channel for the reference device, as predicted from the two-dimensional code.

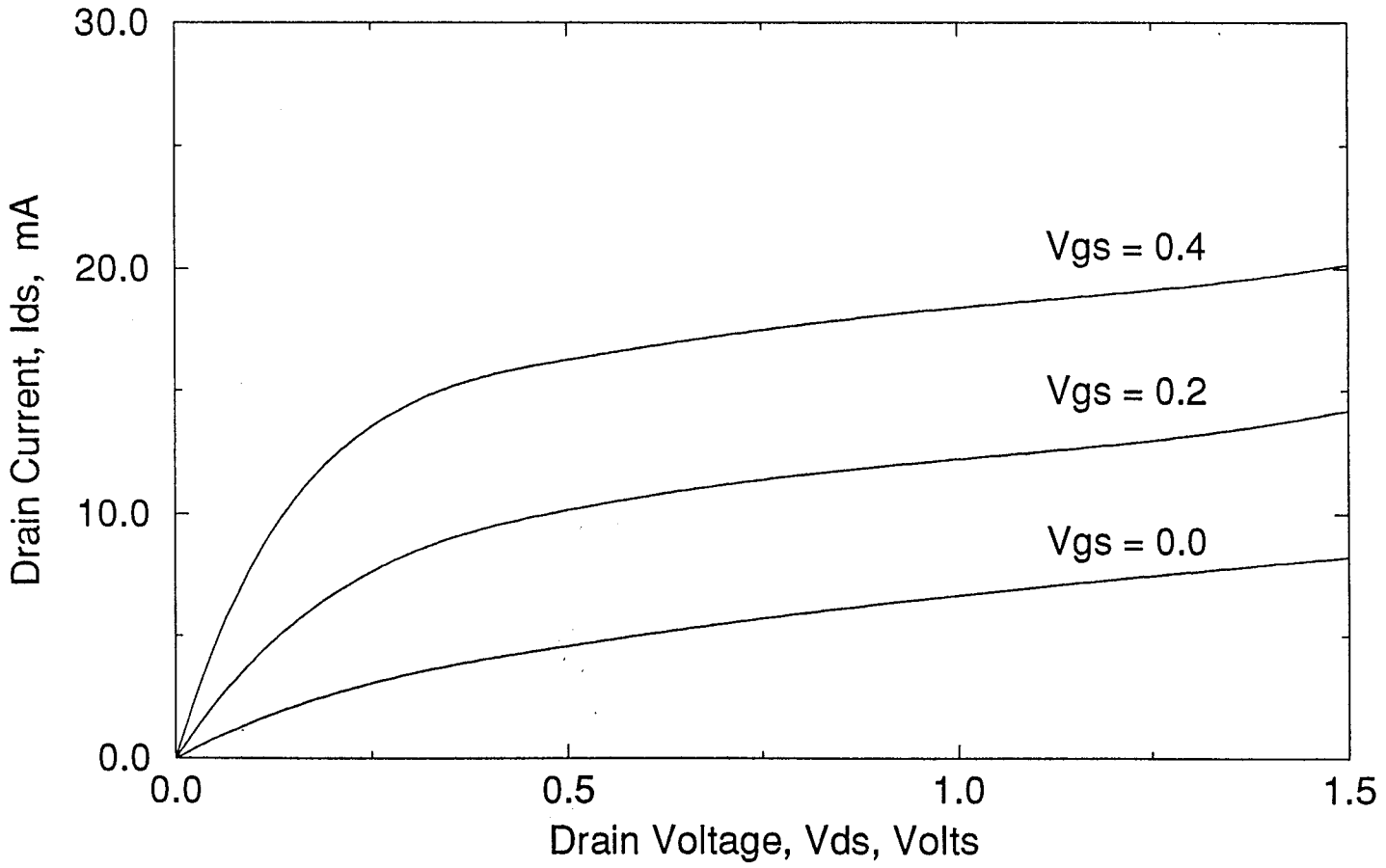
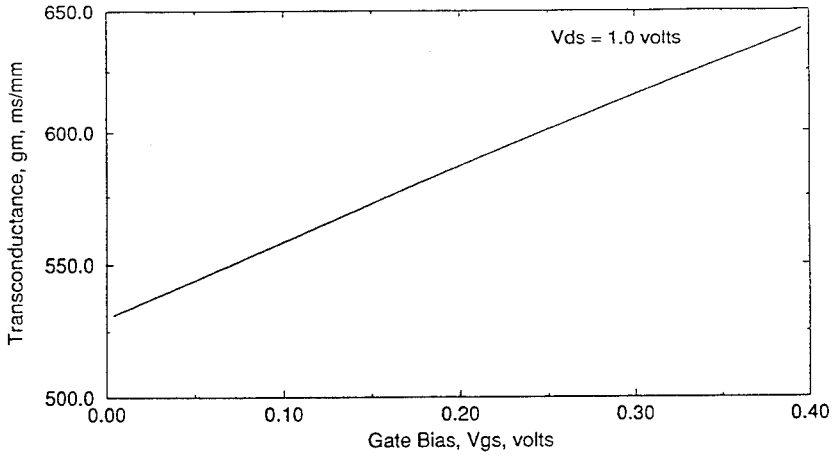
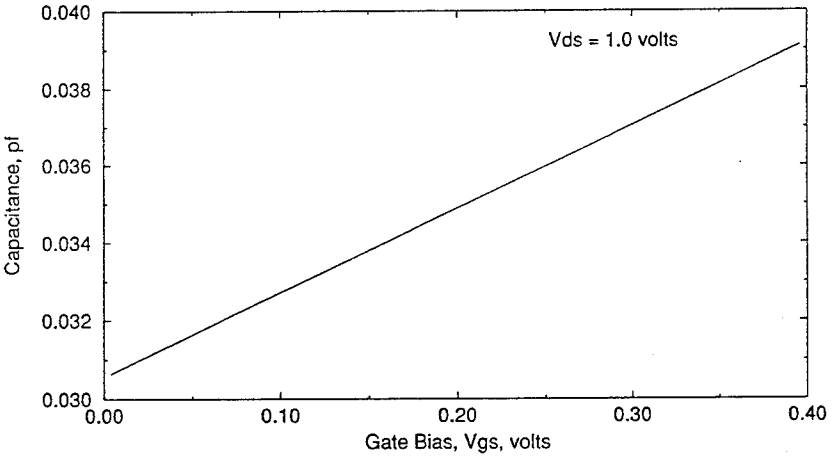


Figure 20. Predicted current-voltage characteristics for a 20% reduction in planar layer doping.





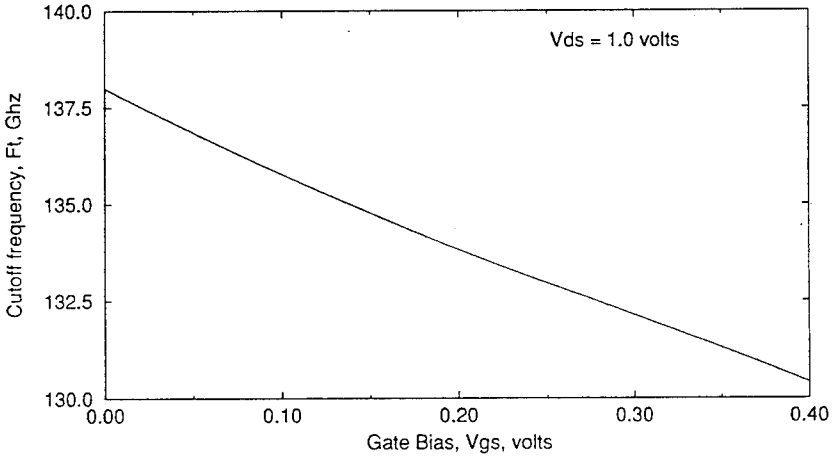


Figure 21. Predicted transconductance, capacitance and cut-off frequency for a 20% reduction in planar layer doping.

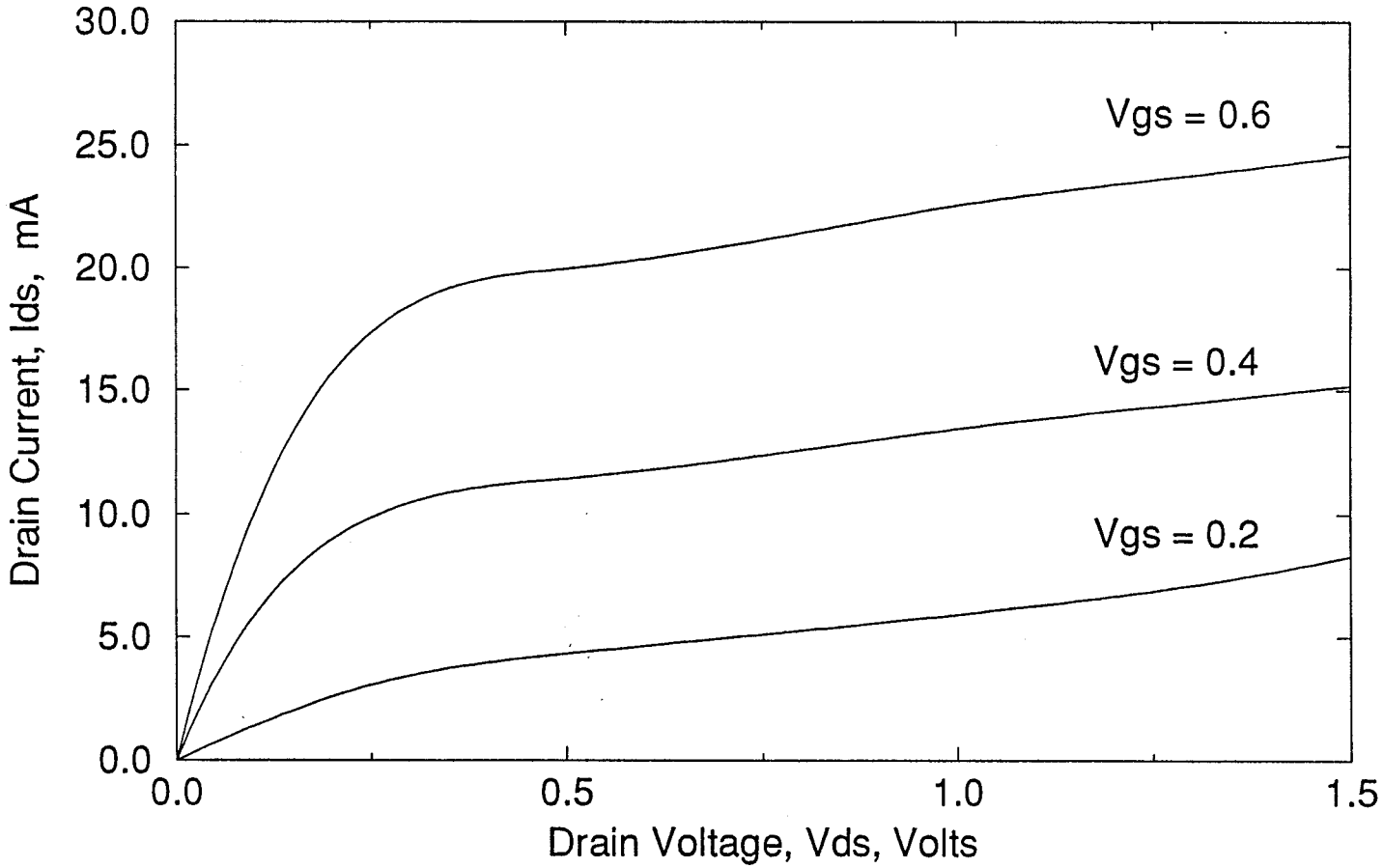
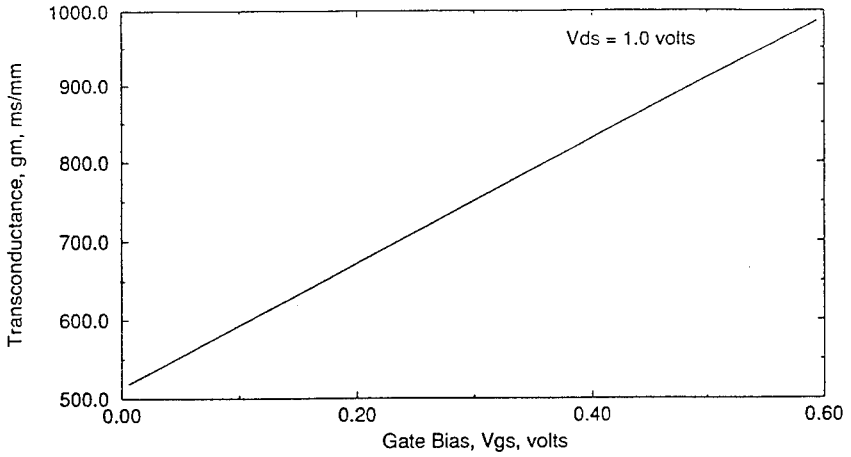
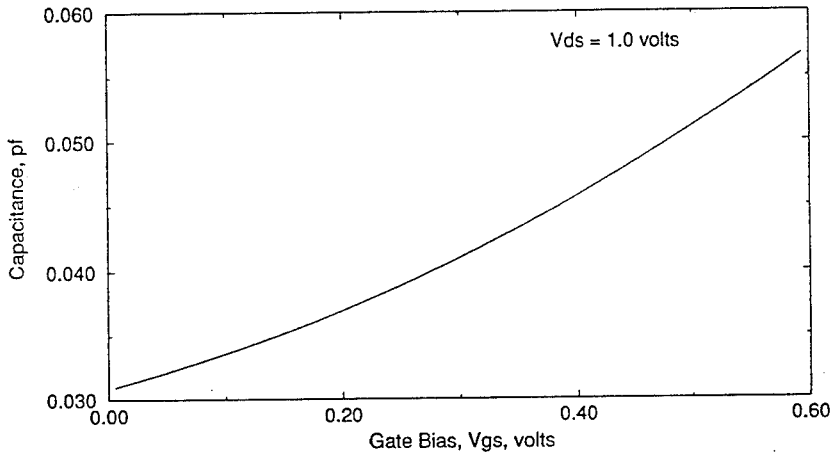


Figure 22. Predicted current-voltage characteristics for an increased gate recess depth.





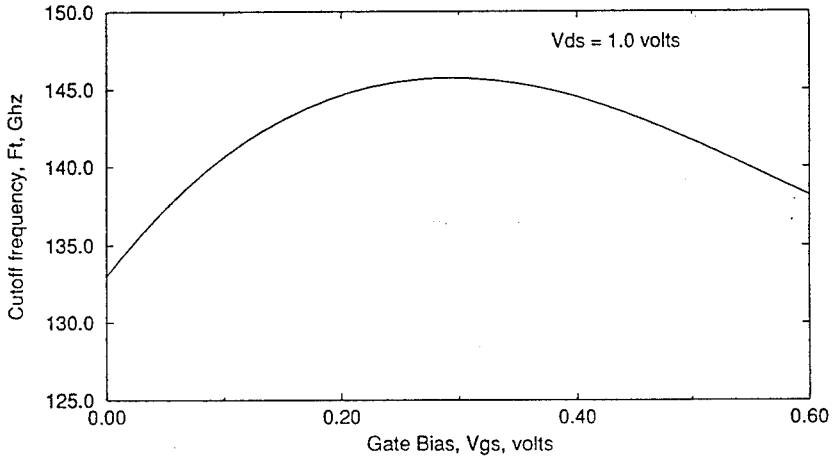


Figure 23. Predicted transconductance, capacitance and cut-off frequency for an increased gate recess depth.

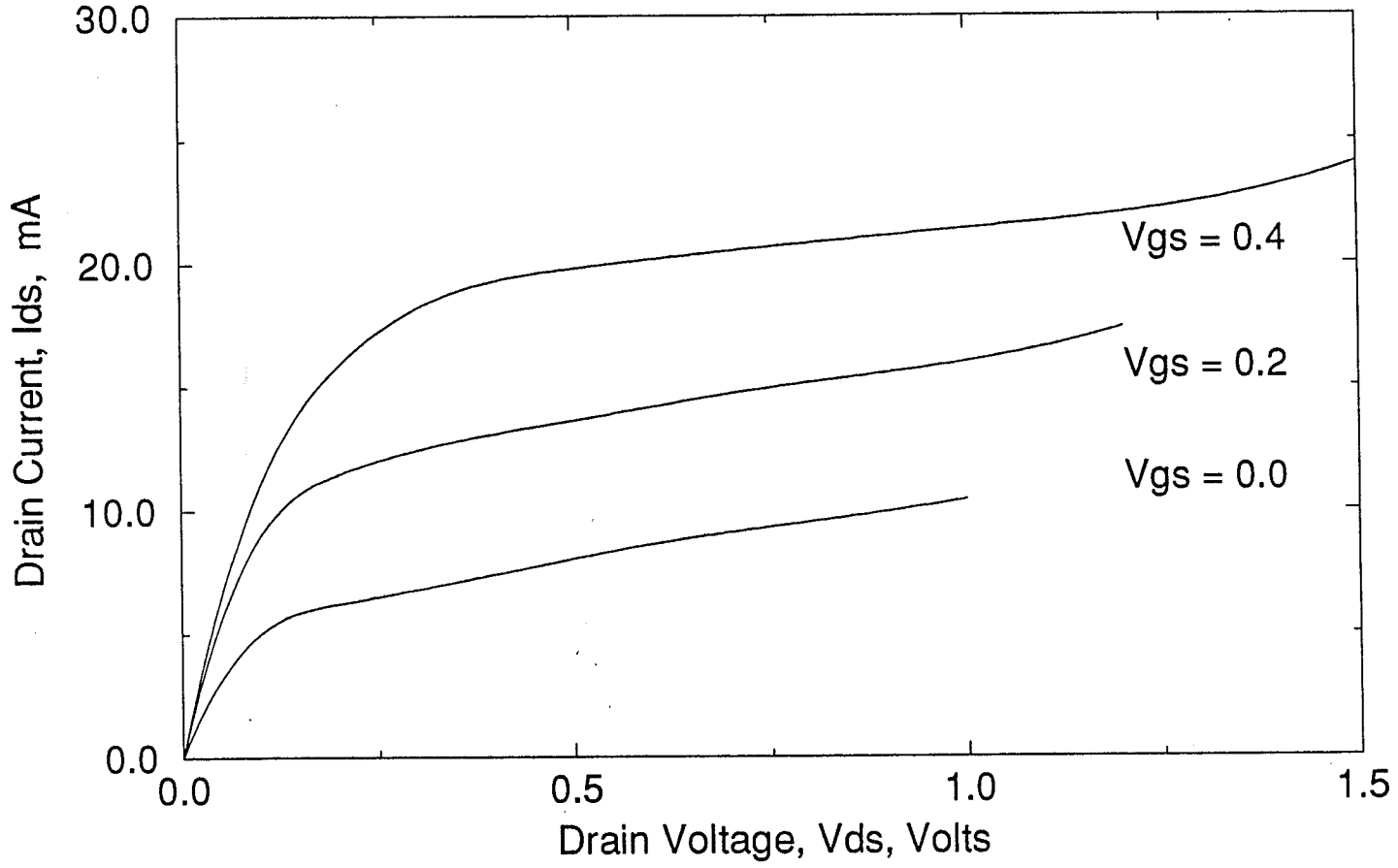
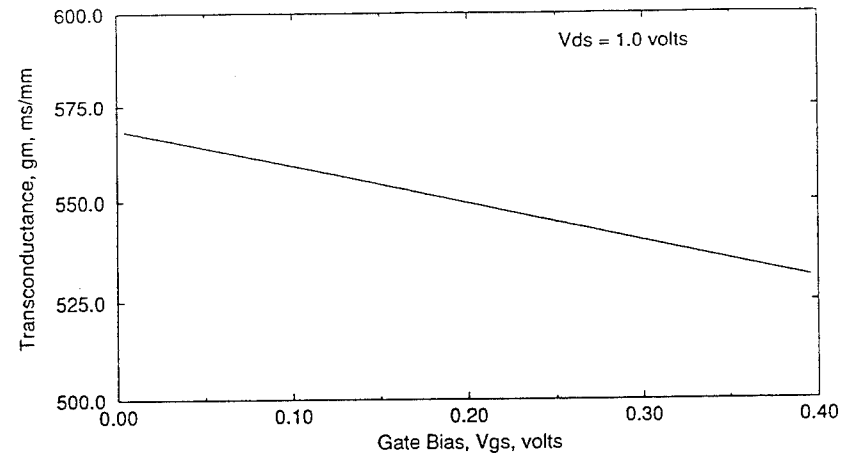
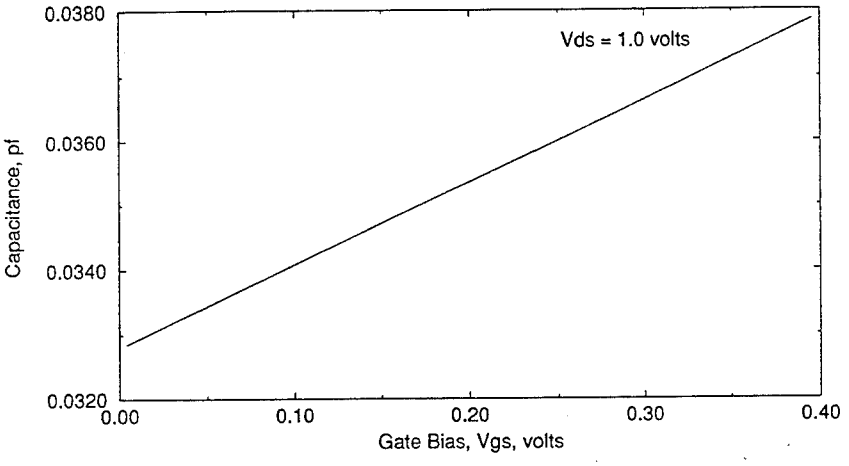


Figure 24. Predicted current-voltage characteristics for an increase in spacer layer thickness.





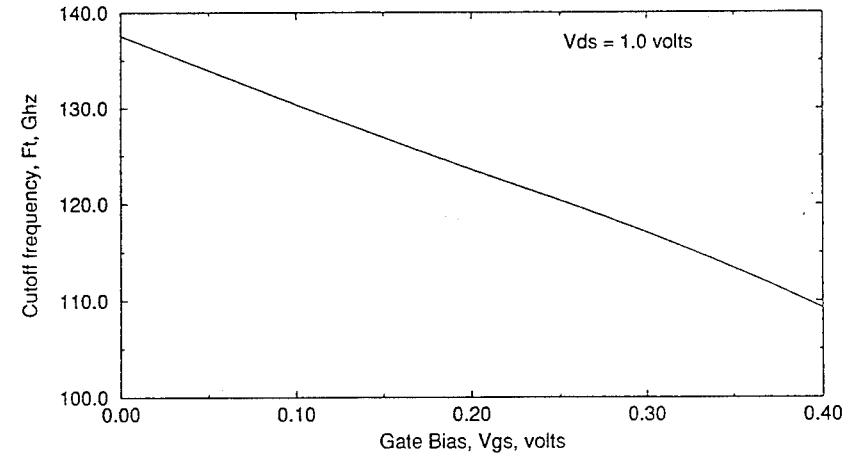


Figure 25. Predicted transconductance, capacitance and cut-off frequency for an increase in spacer layer thickness.

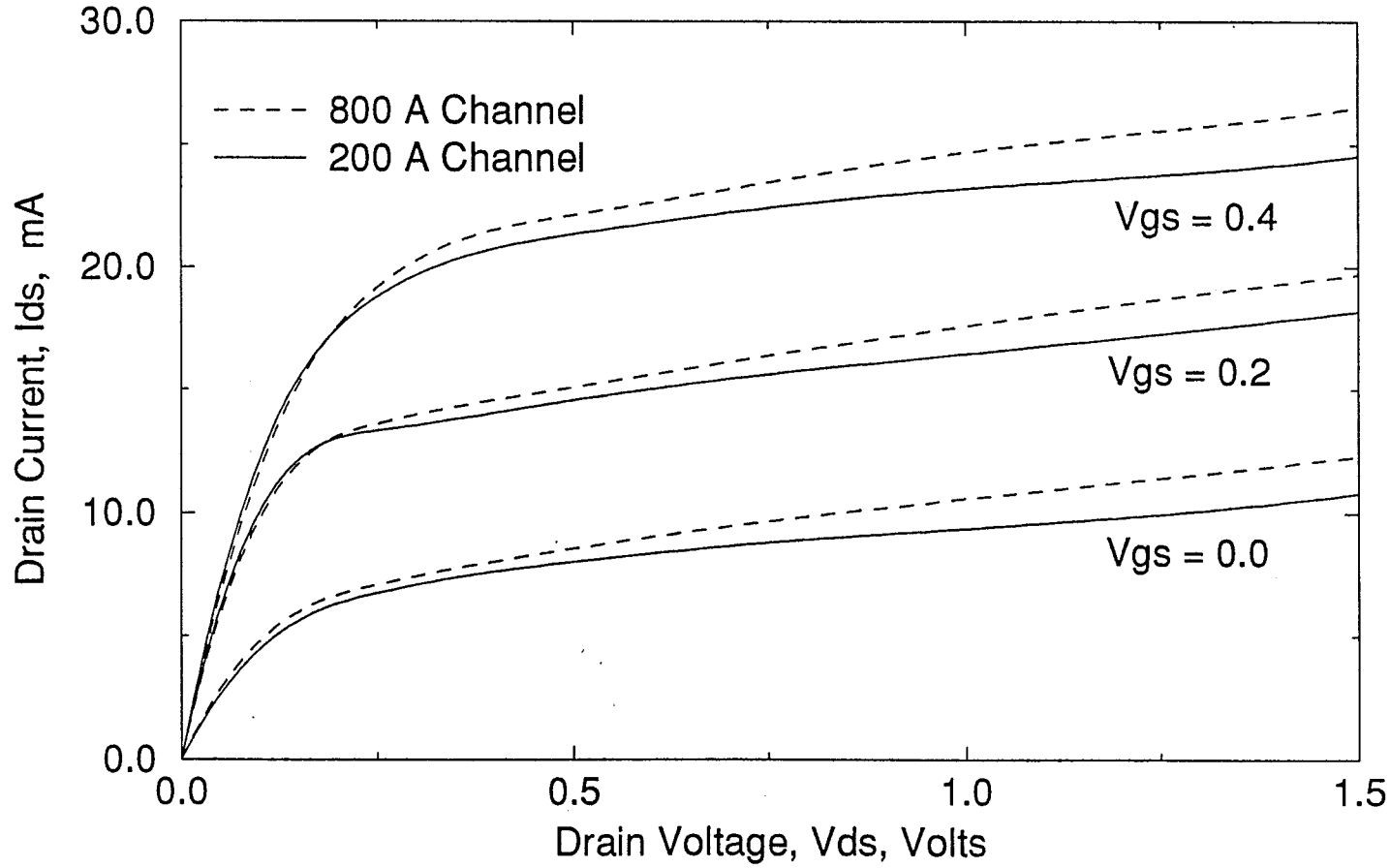
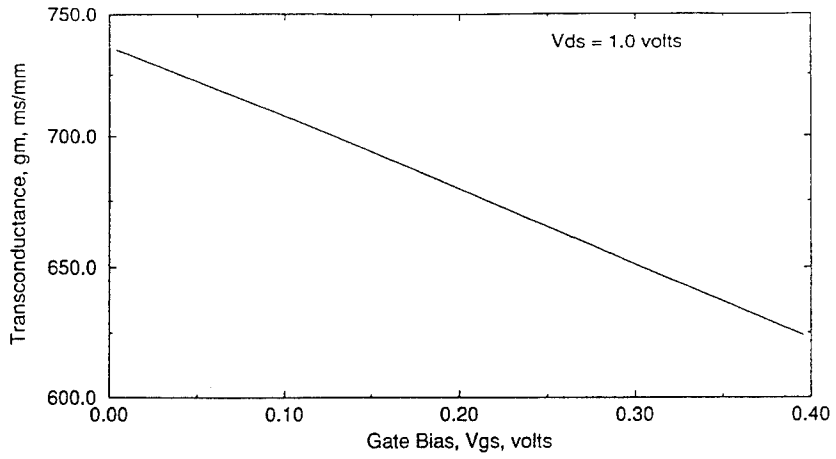
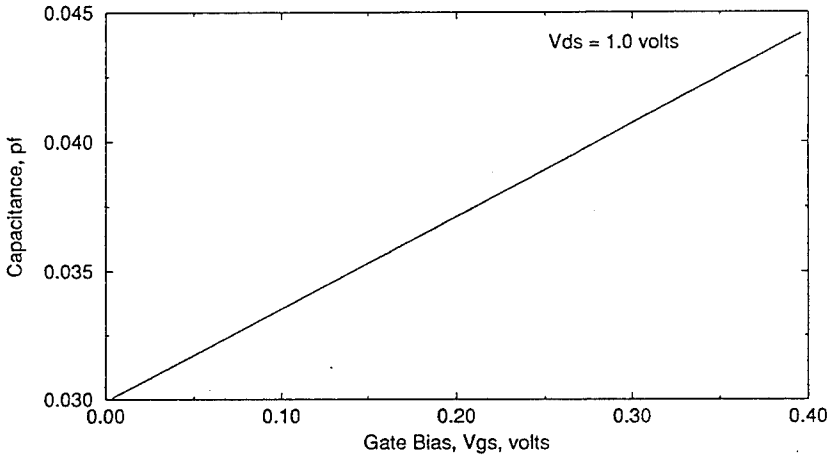


Figure 26. Predicted current-voltage characteristics for a reduction in channel depth.





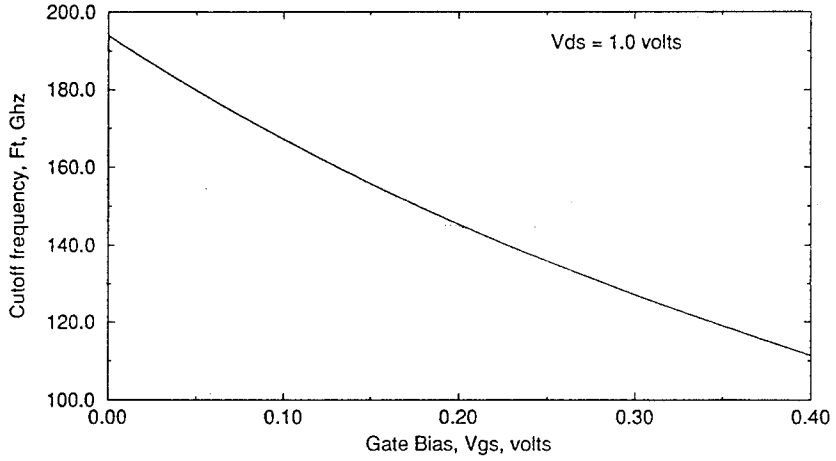


Figure 27. Predicted transconductance, capacitance and cut-off frequency for a reduction in channel depth.

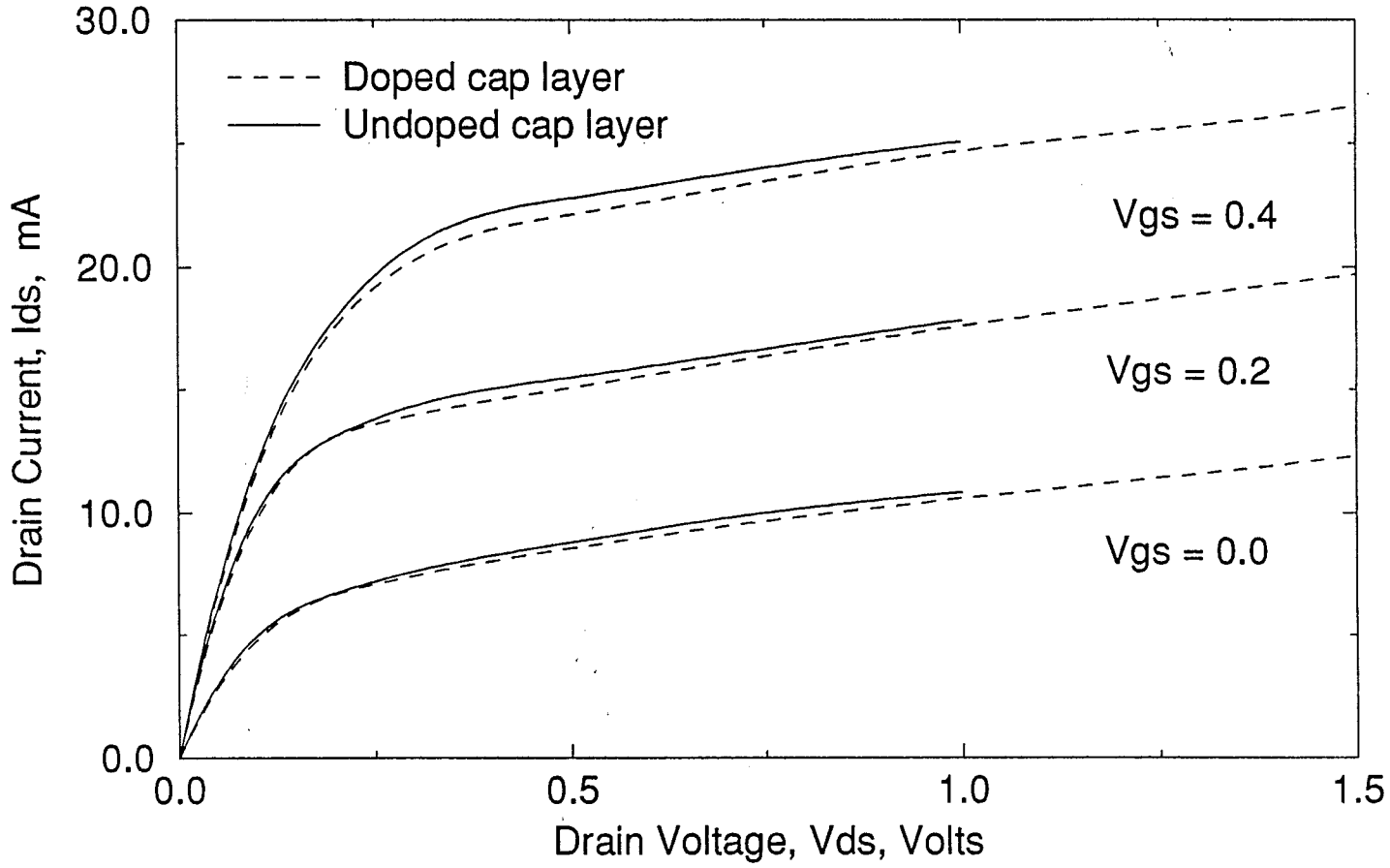
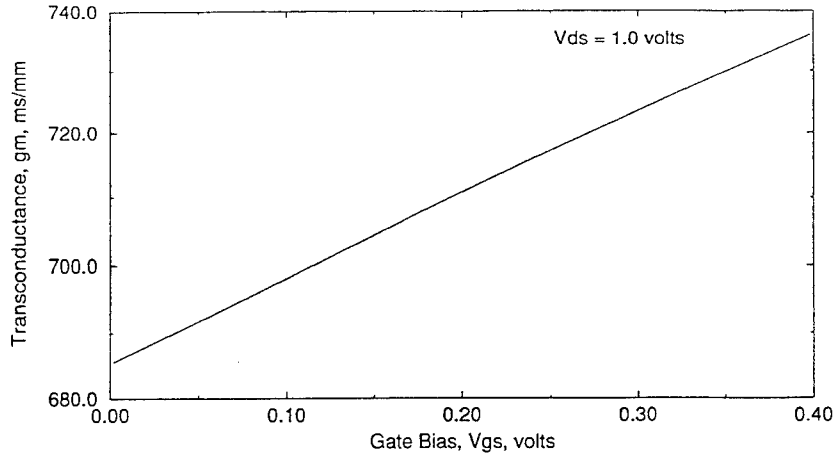
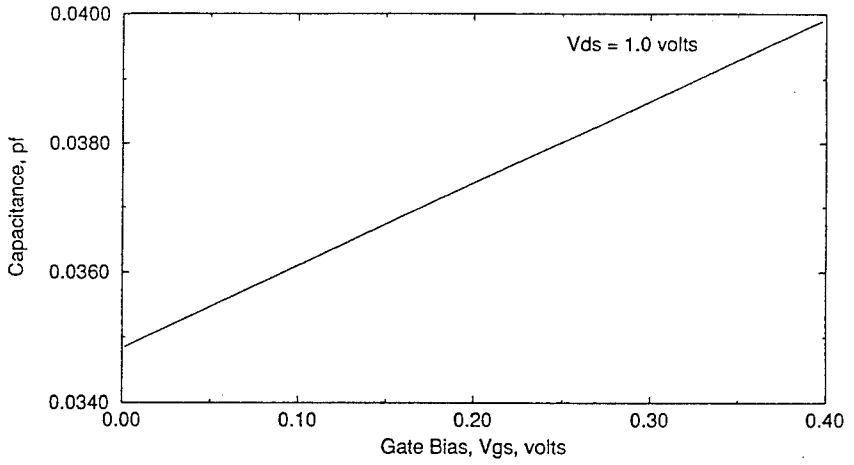


Figure 28. Predicted current-voltage characteristics for a device with an undoped cap layer.





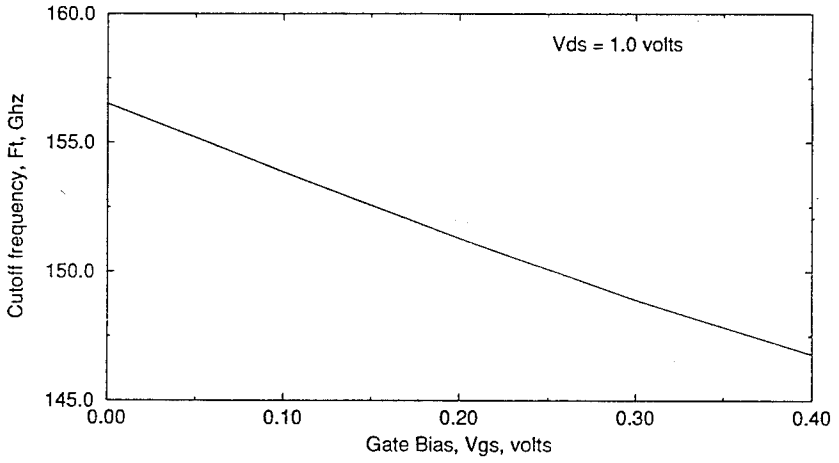
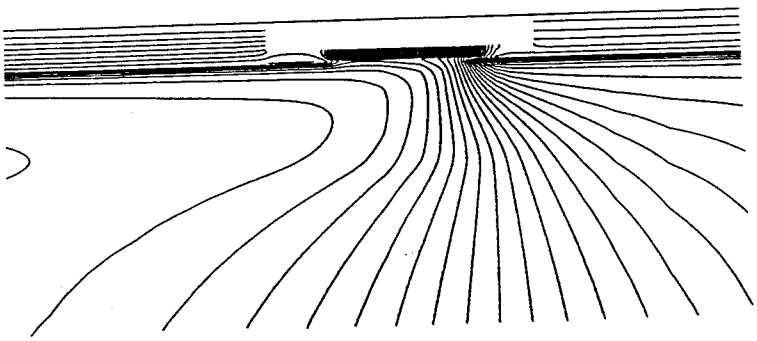


Figure 29. Predicted transconductance, capacitance and cut-off frequency for a device with an undoped cap layer.

a) doped cap layer



b) undoped cap layer

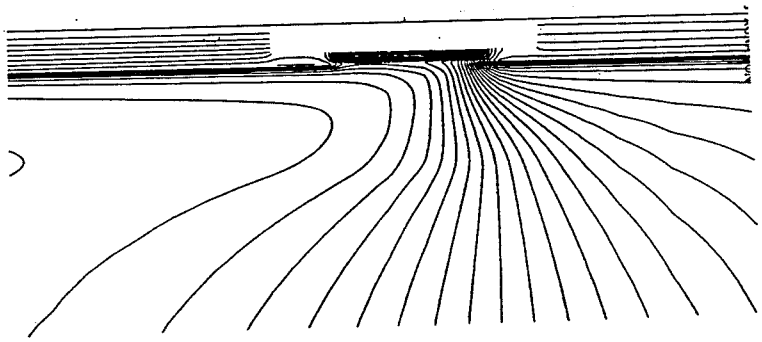


Figure 30. Comparison of potential distributions around the gate for the reference device and the device with an undoped cap layer.

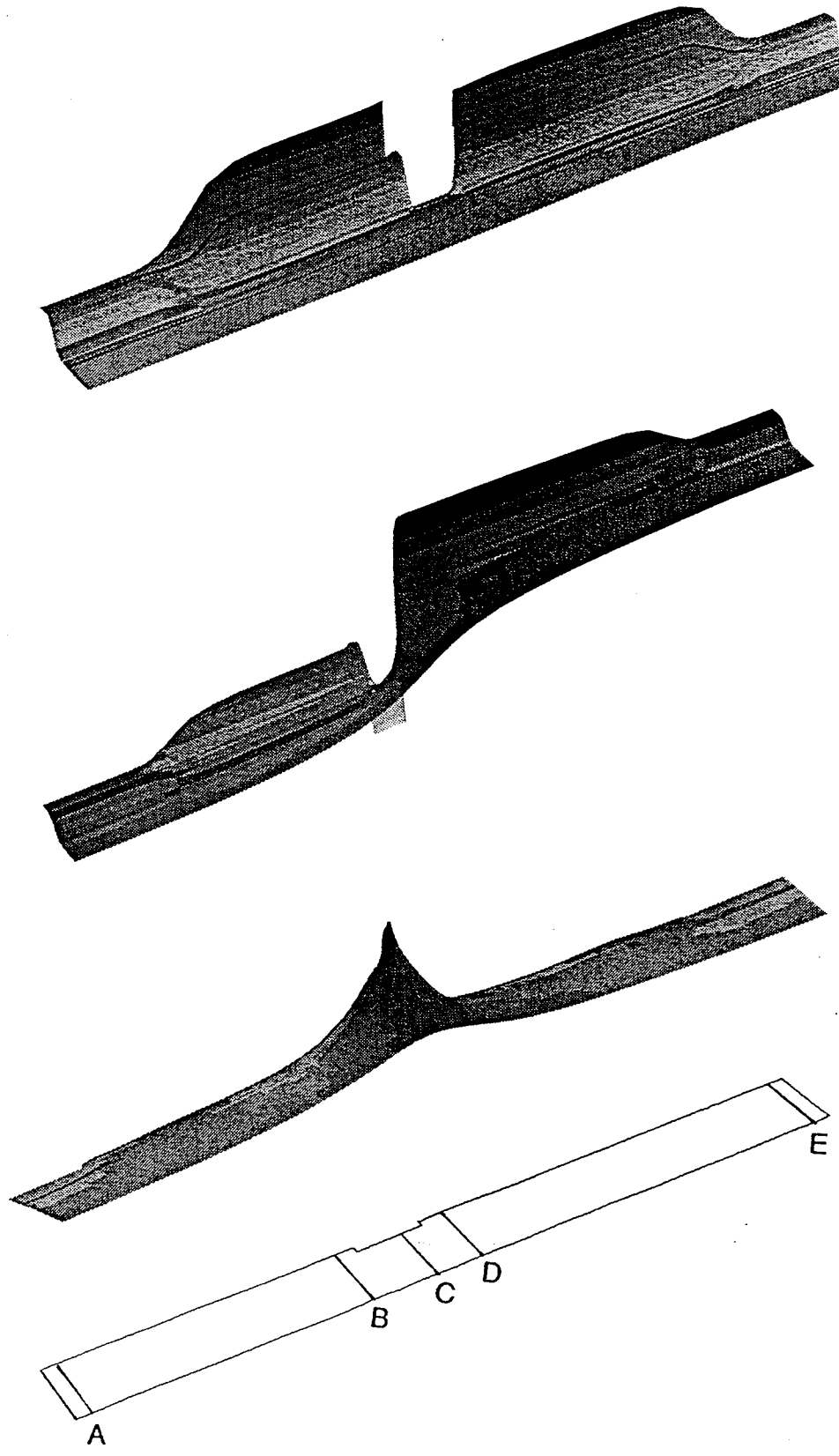


Figure 31. Surface plots of density, potential and electron temperature for the initially simulated device with a uniformly doped isolation layer.

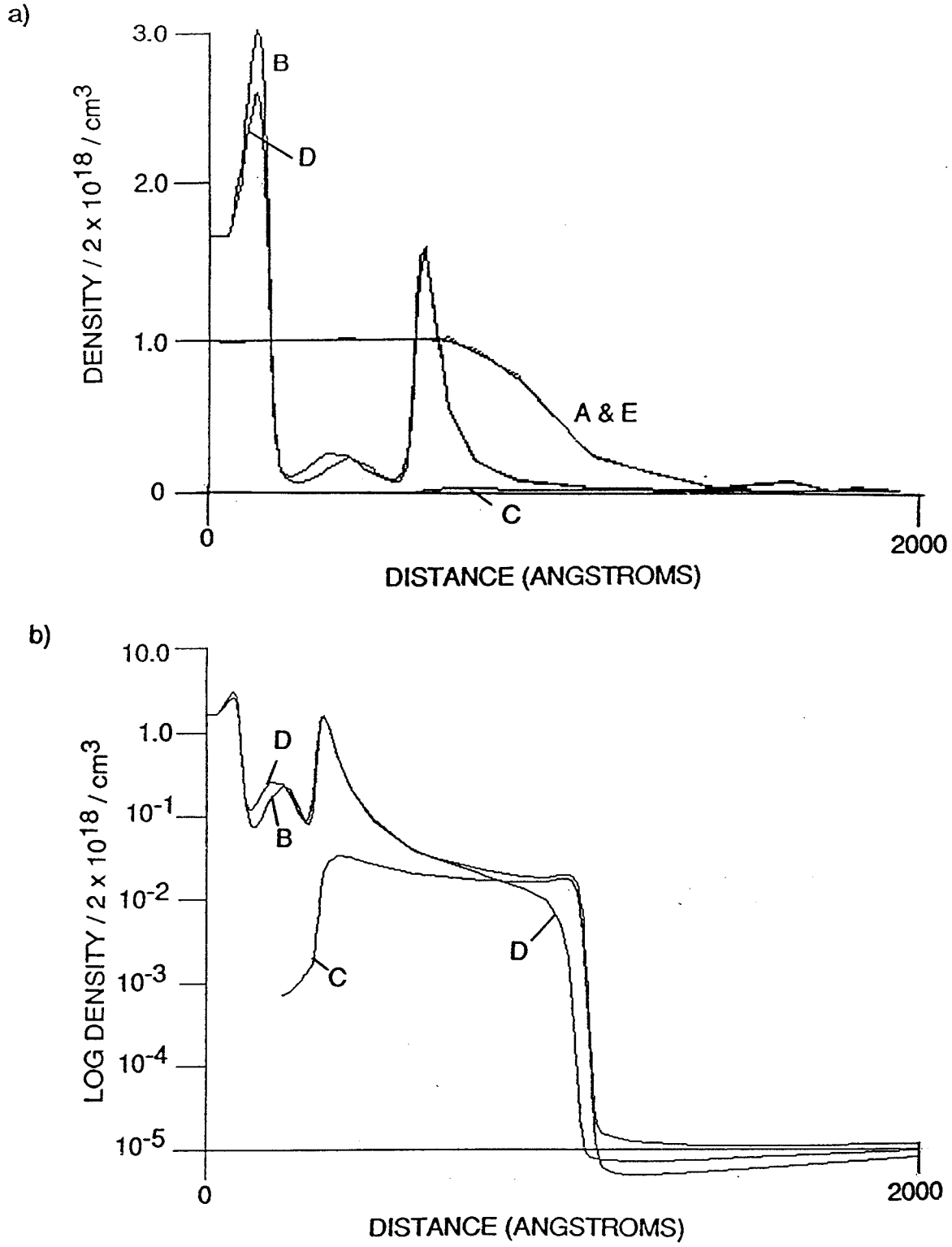


Figure 32. Density distribution along planes normal to the device surface at the positions denoted in Figure 31.

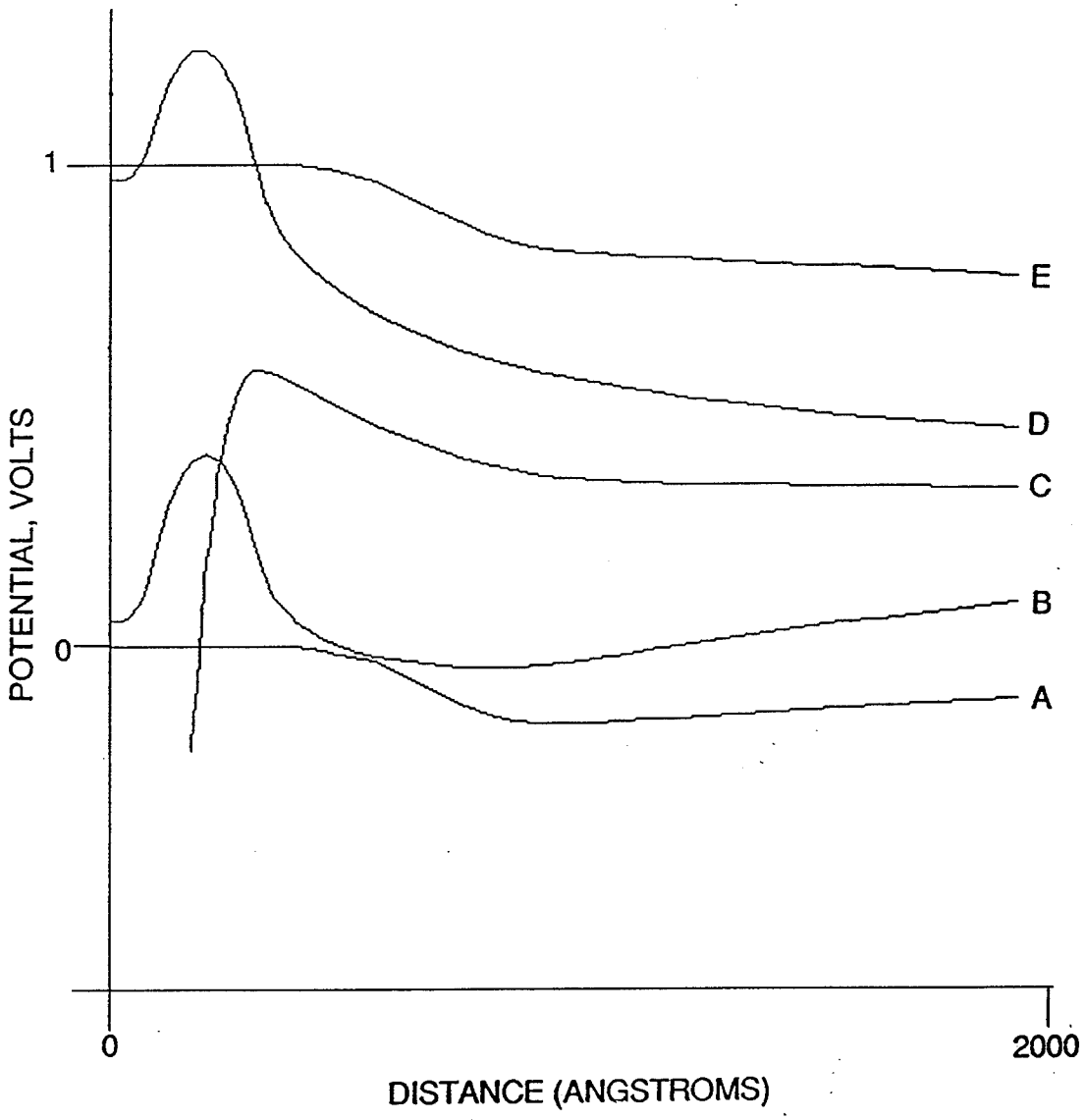


Figure 33. Similar to Figure 32 but for potential.

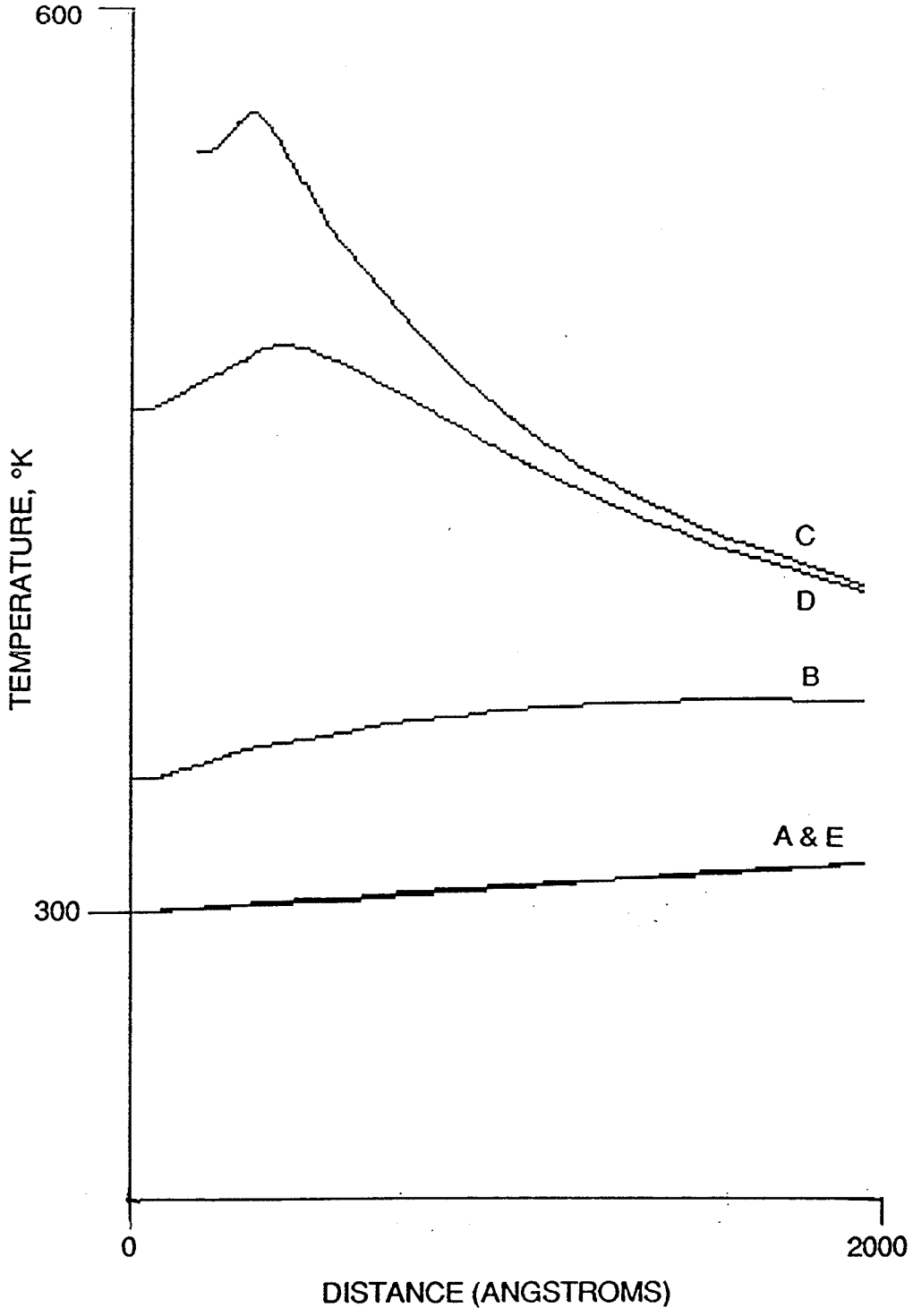


Figure 34. Similar to Figure 32 but for temperature.

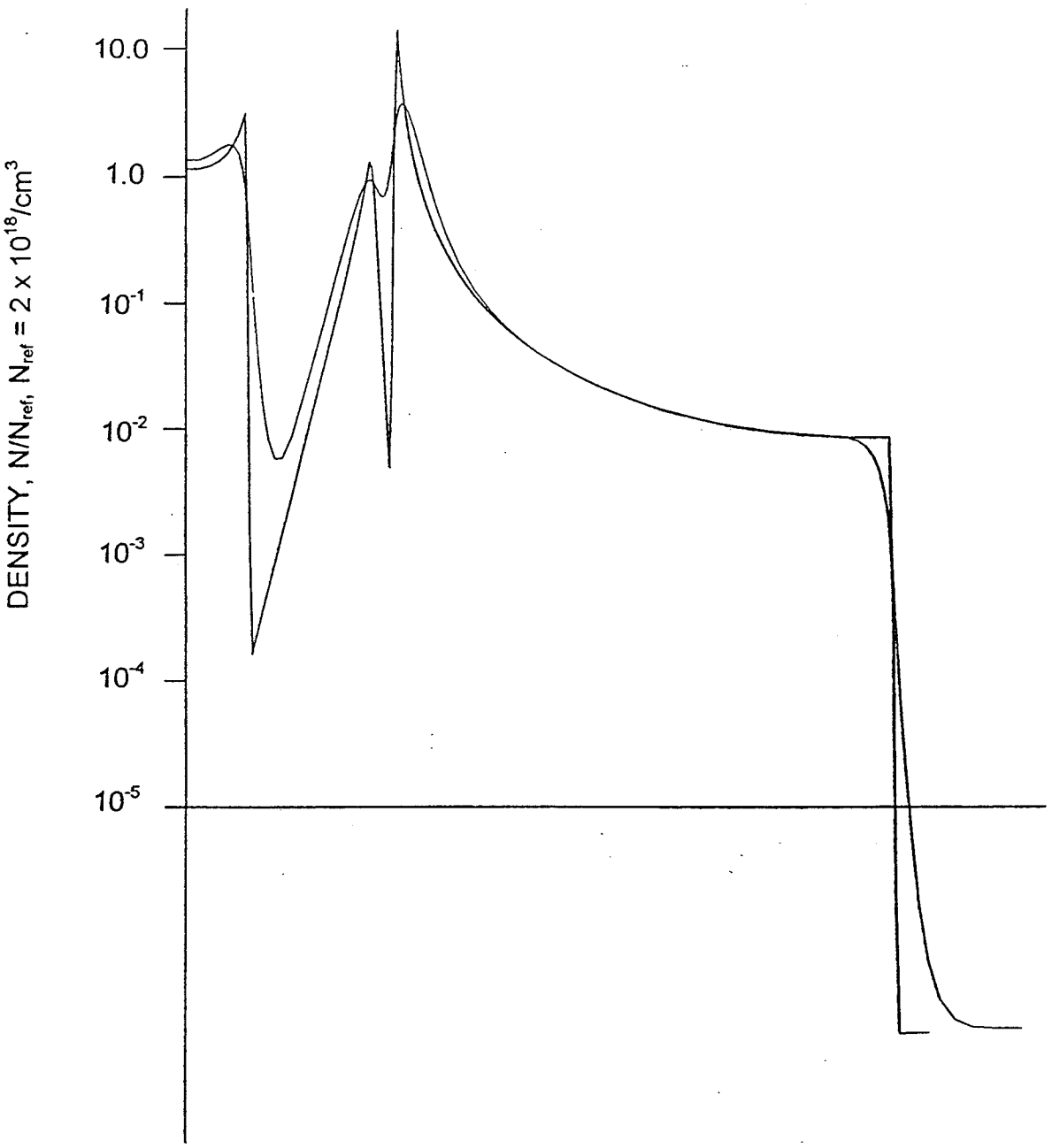


Figure 35. Comparison of the density distribution across the reference device structure, under the cap layer, as computed from classical and quantum-hydrodynamics codes.

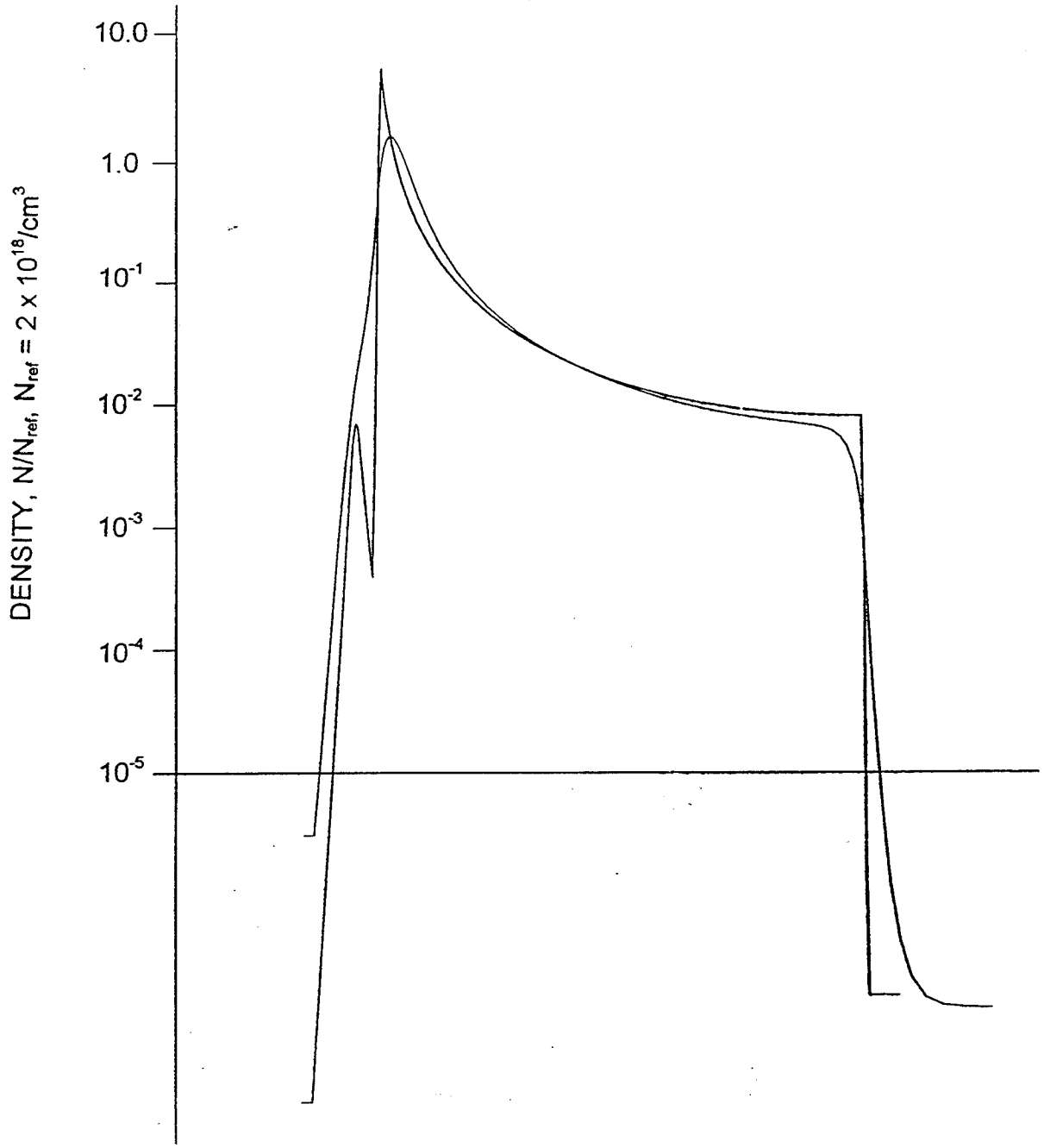


Figure 36. Similar to Figure 35 but under the gate.

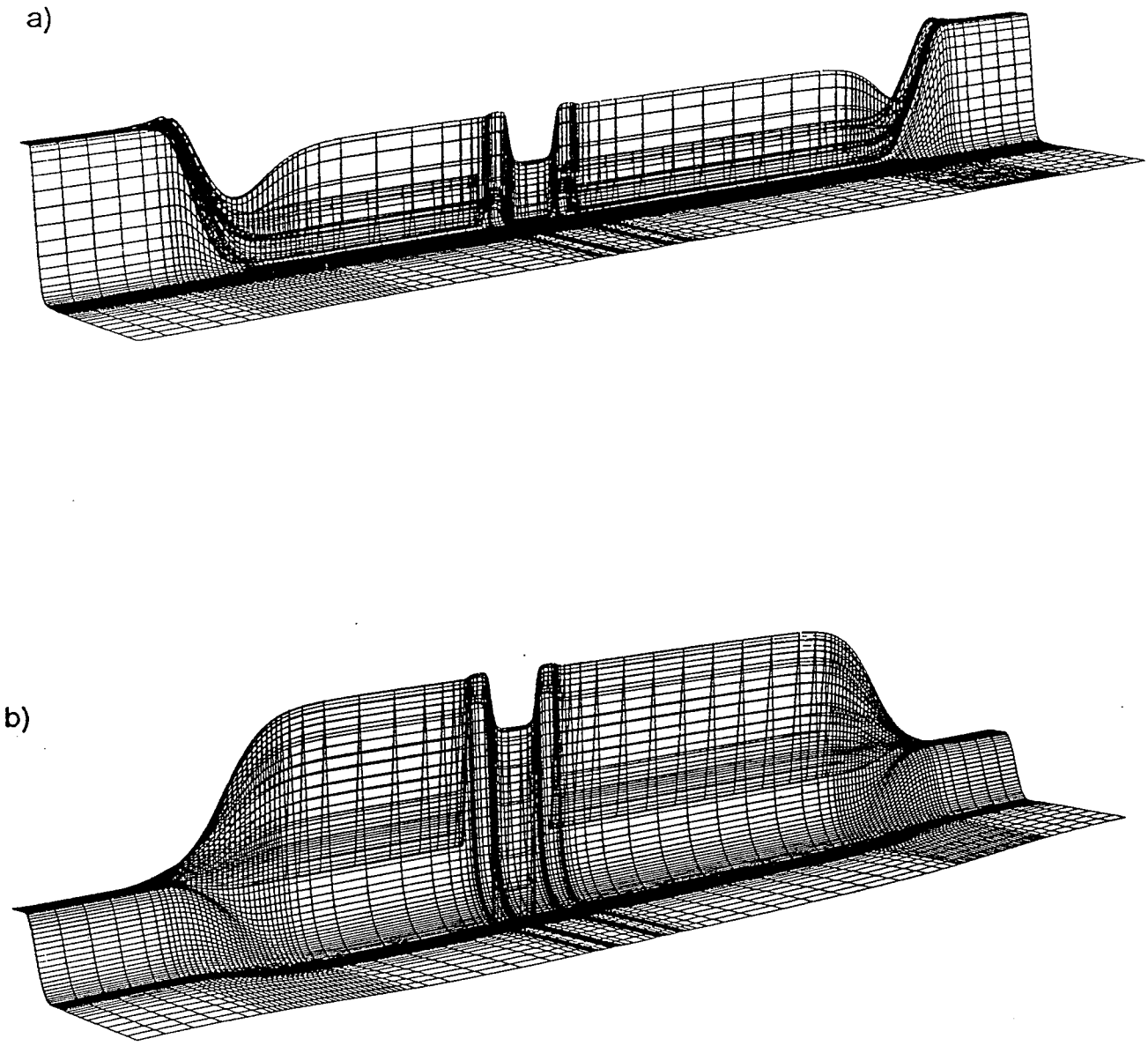


Figure 37. Surface plots of the zero bias a) density and b) potential for the reference device structure.

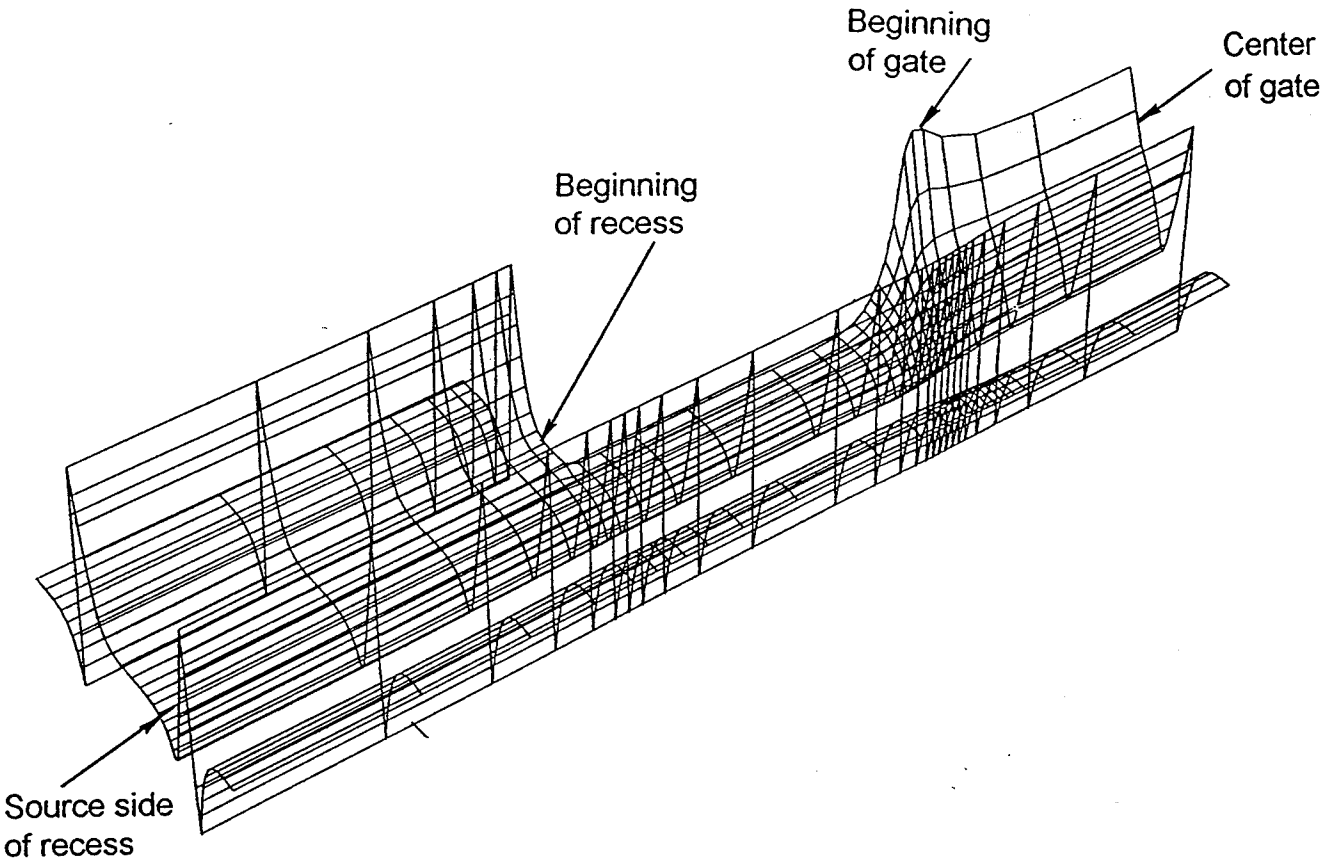


Figure 38. Enlargement of the surface plot of the quantum potential surrounding the gate recess at zero bias.

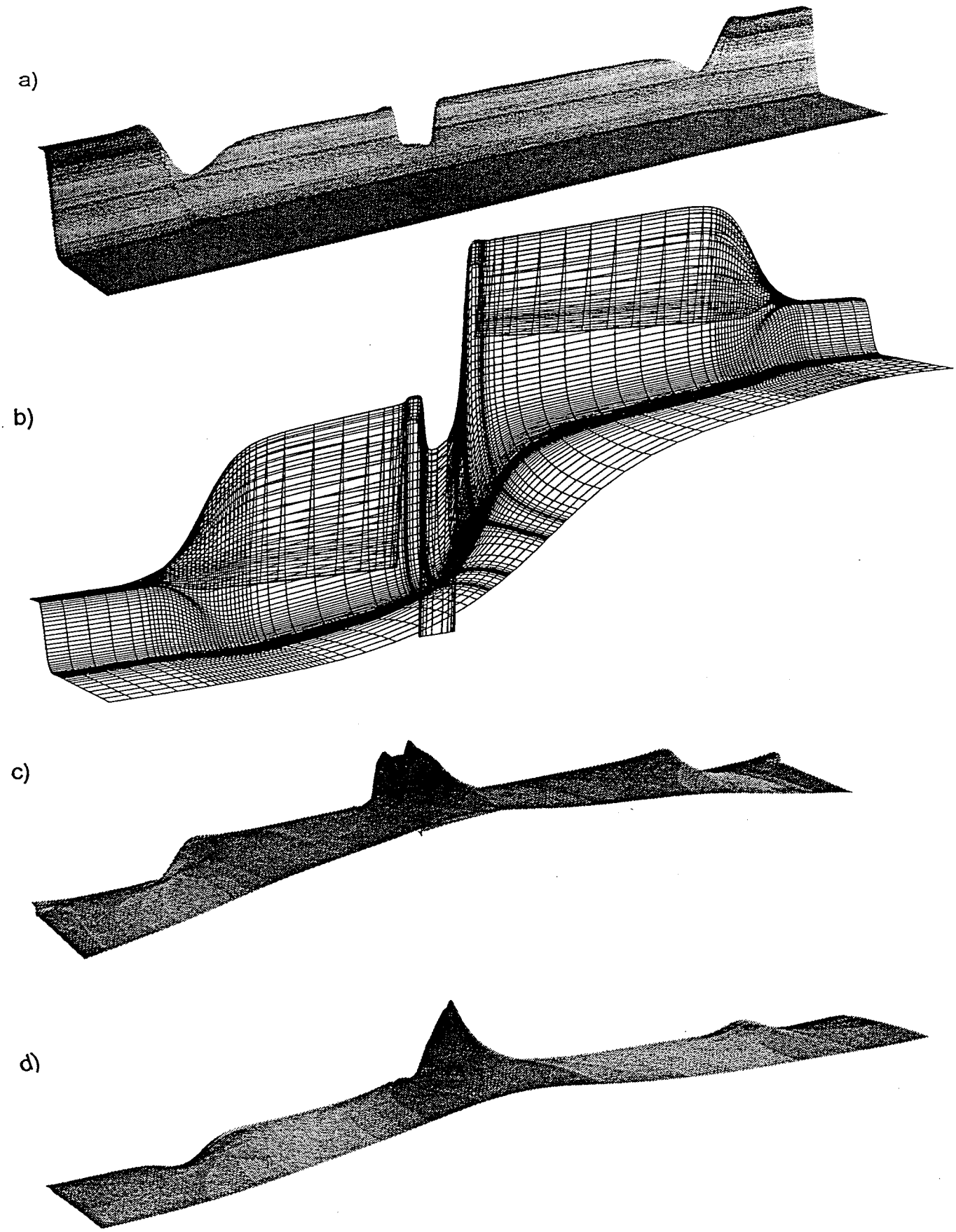


Figure 39. Surface plots of a) density, b) potential, c) velocity and d) temperature for the reference device structure at $V_{ds} = 0.5$ and $V_{gs} = 0.4$ volts.

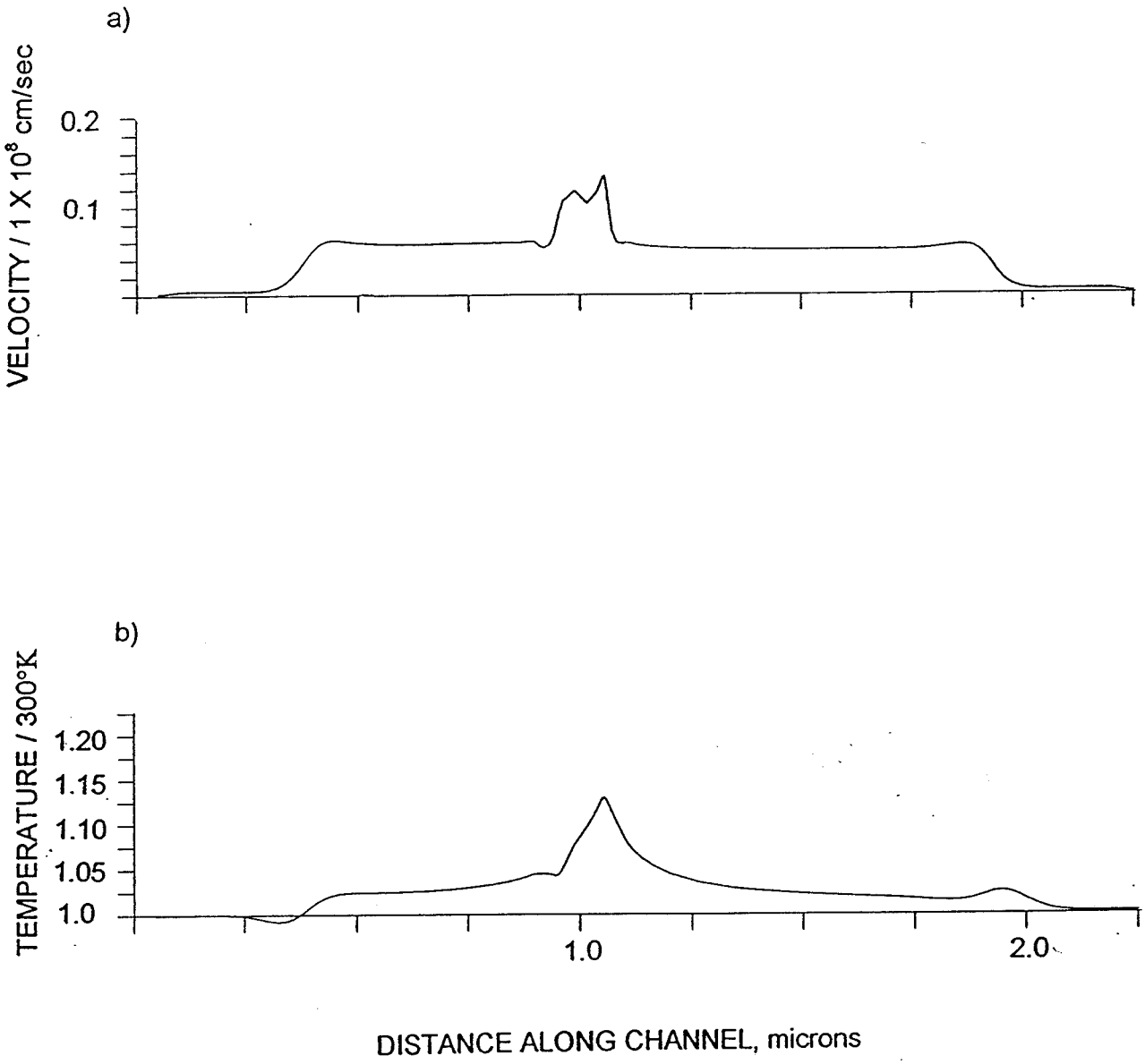


Figure 40. Distribution of velocity and temperature in the plane of maximum density of the 2-DEG as a function of distance along the channel.

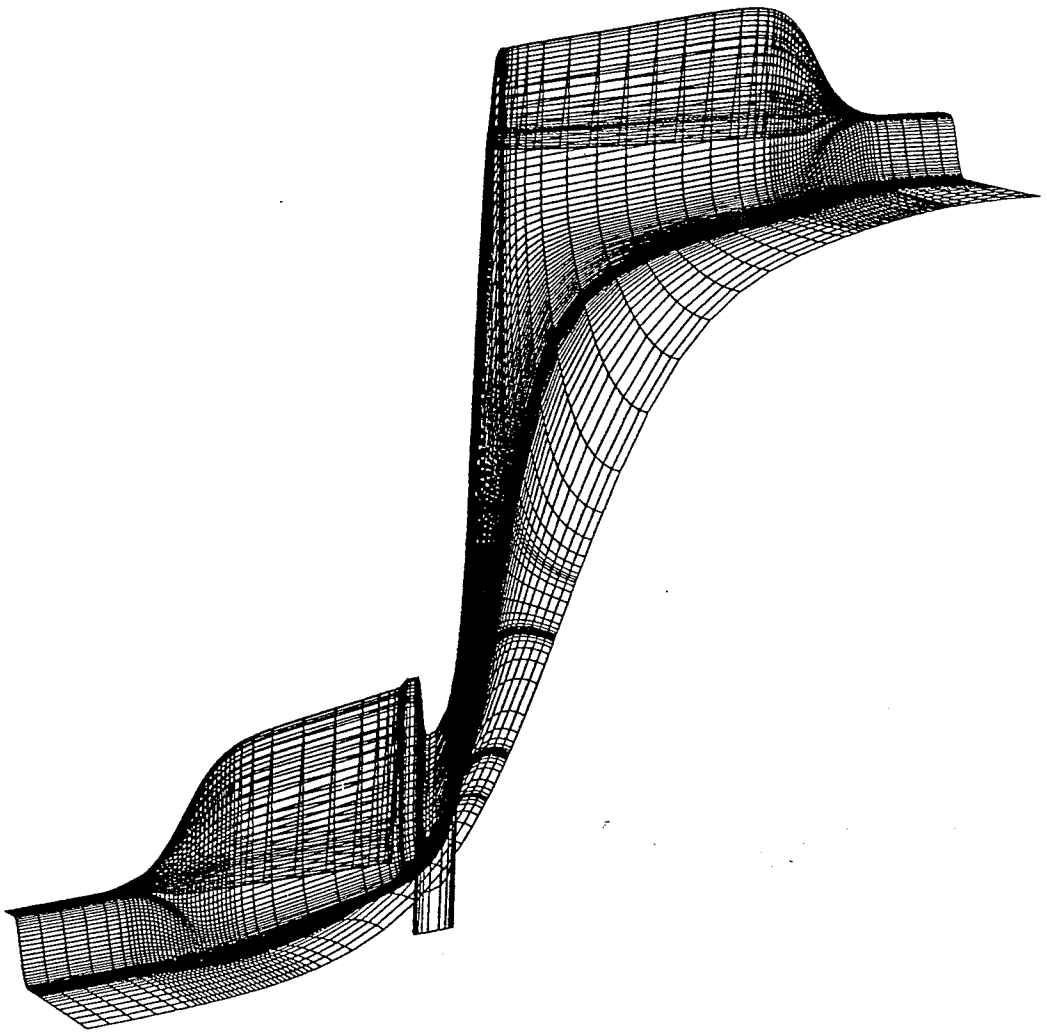


Figure 41. Potential distribution at V_{ds} = 1.5 and V_{gs} = 0.4 volts.

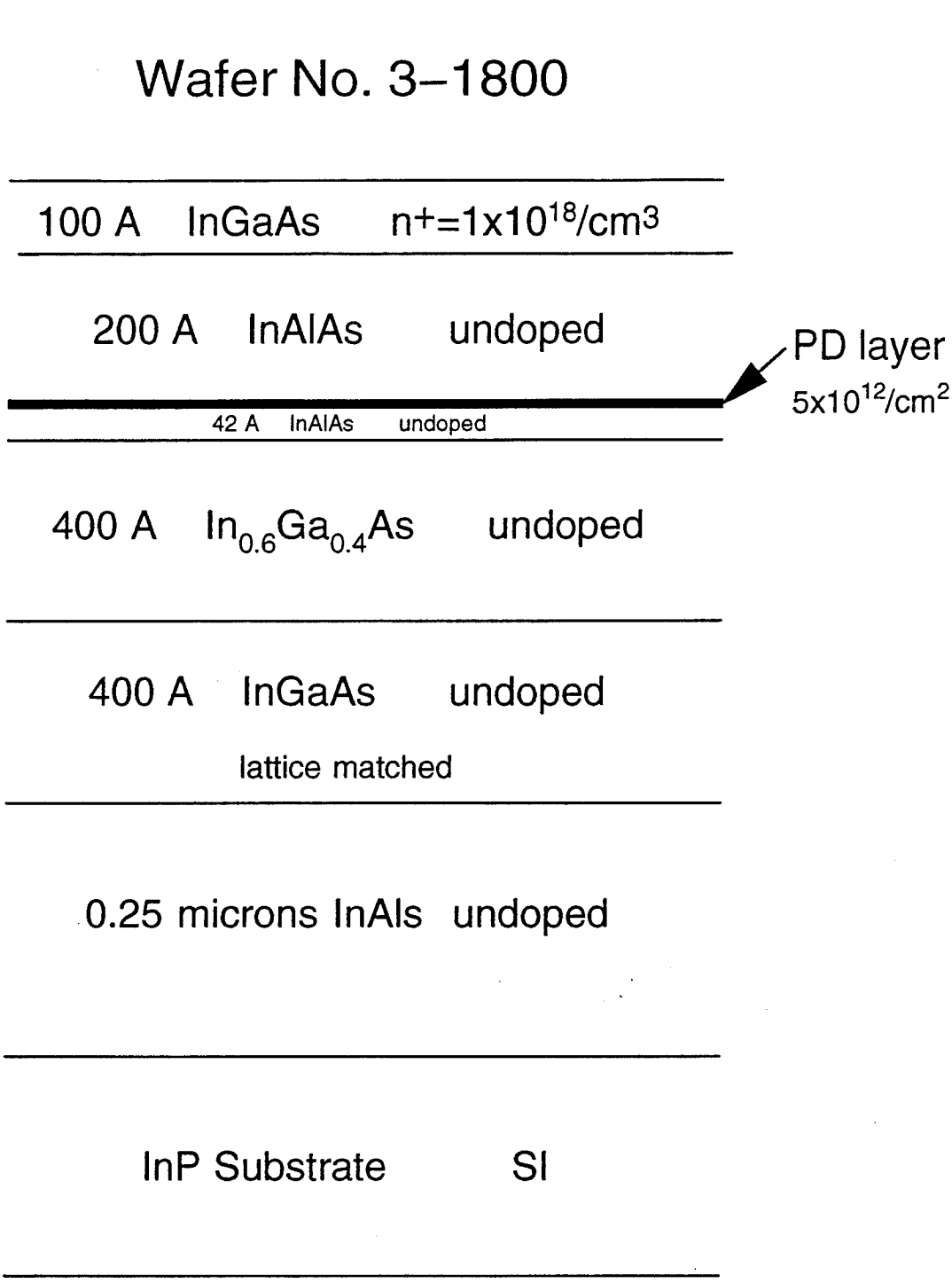


Figure 42. Structure for wafer no. 3-1800.

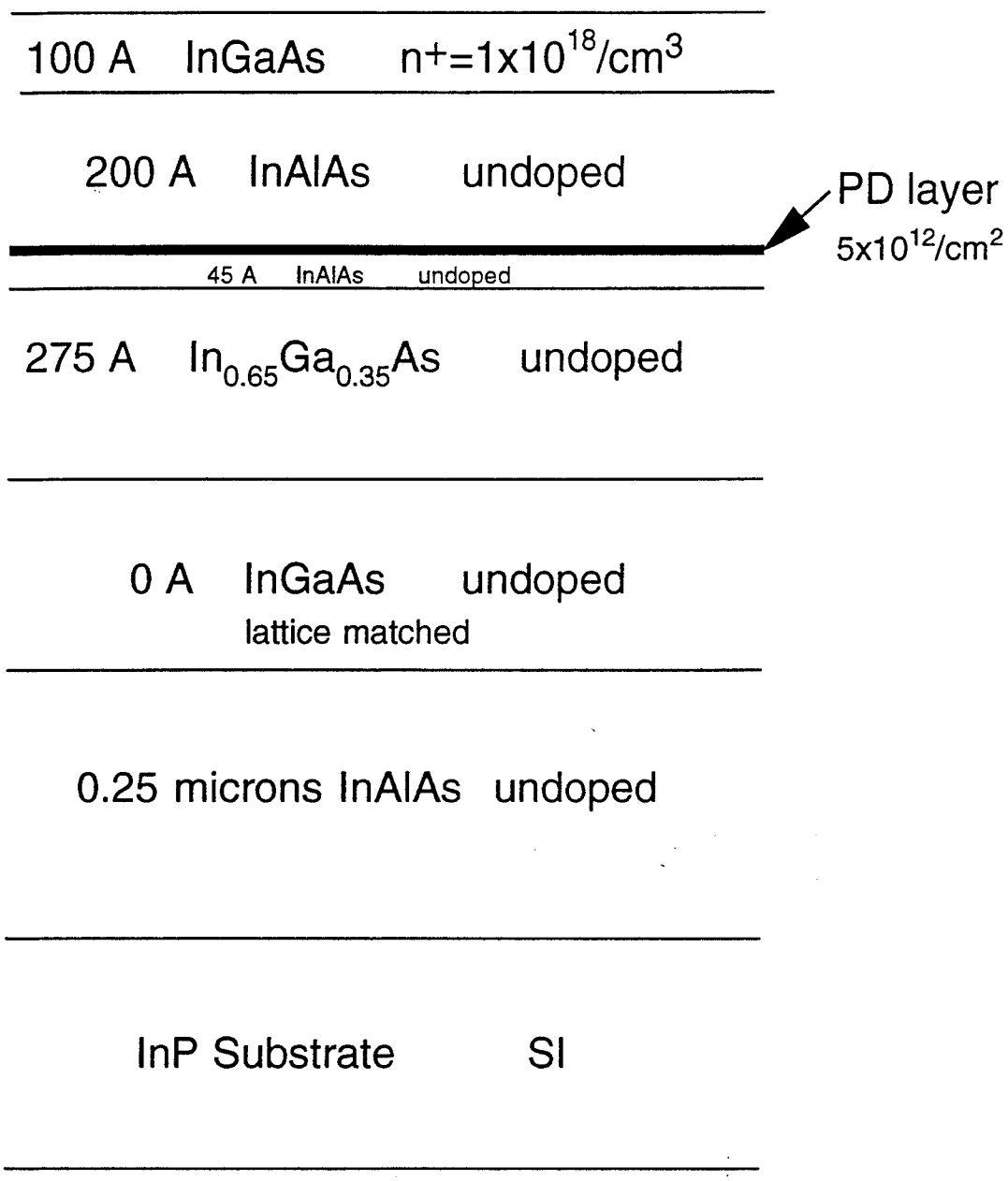


Figure 43. Structure for wafer no. 3-1603.

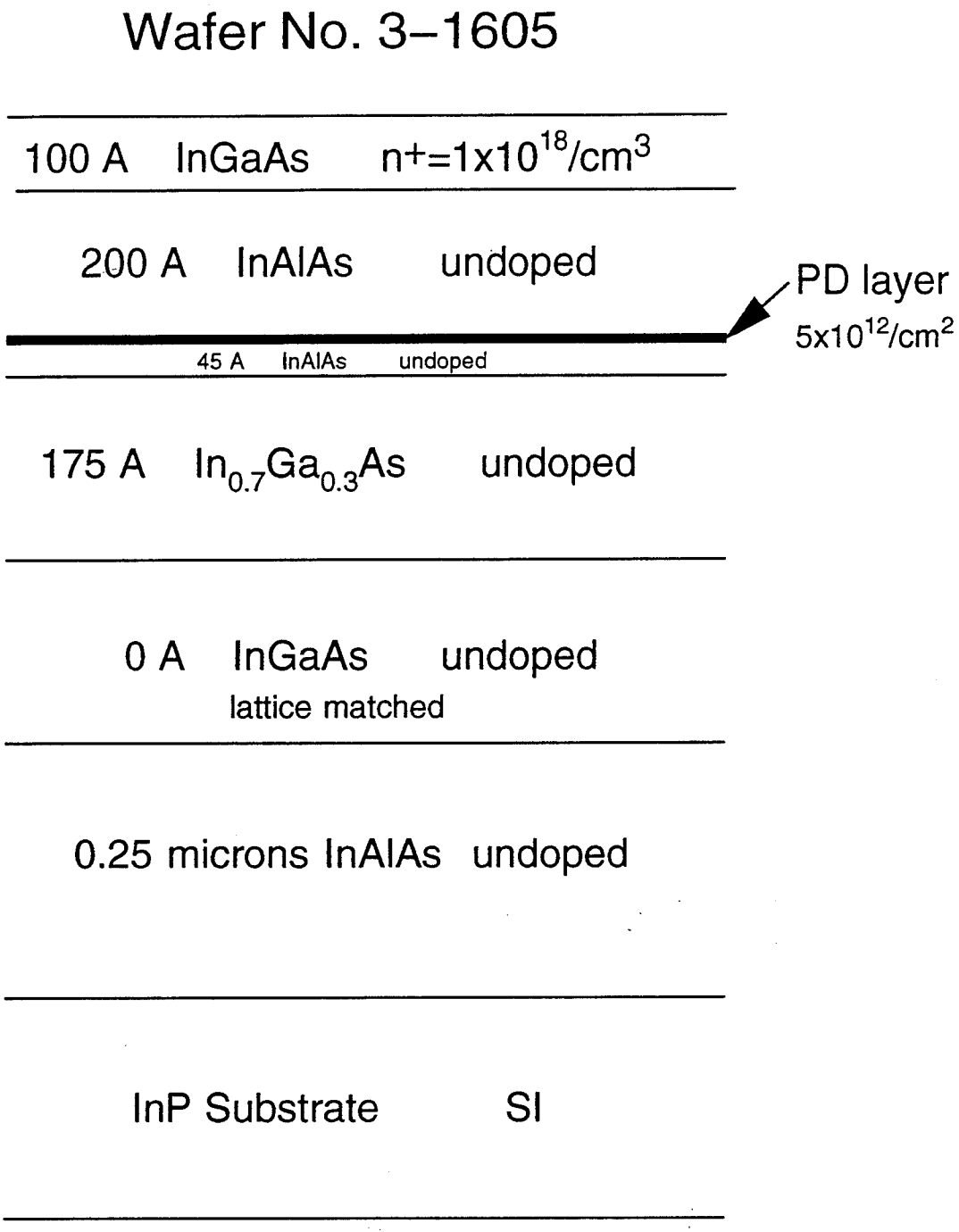


Figure 44. Structure for wafer no. 3-1605.

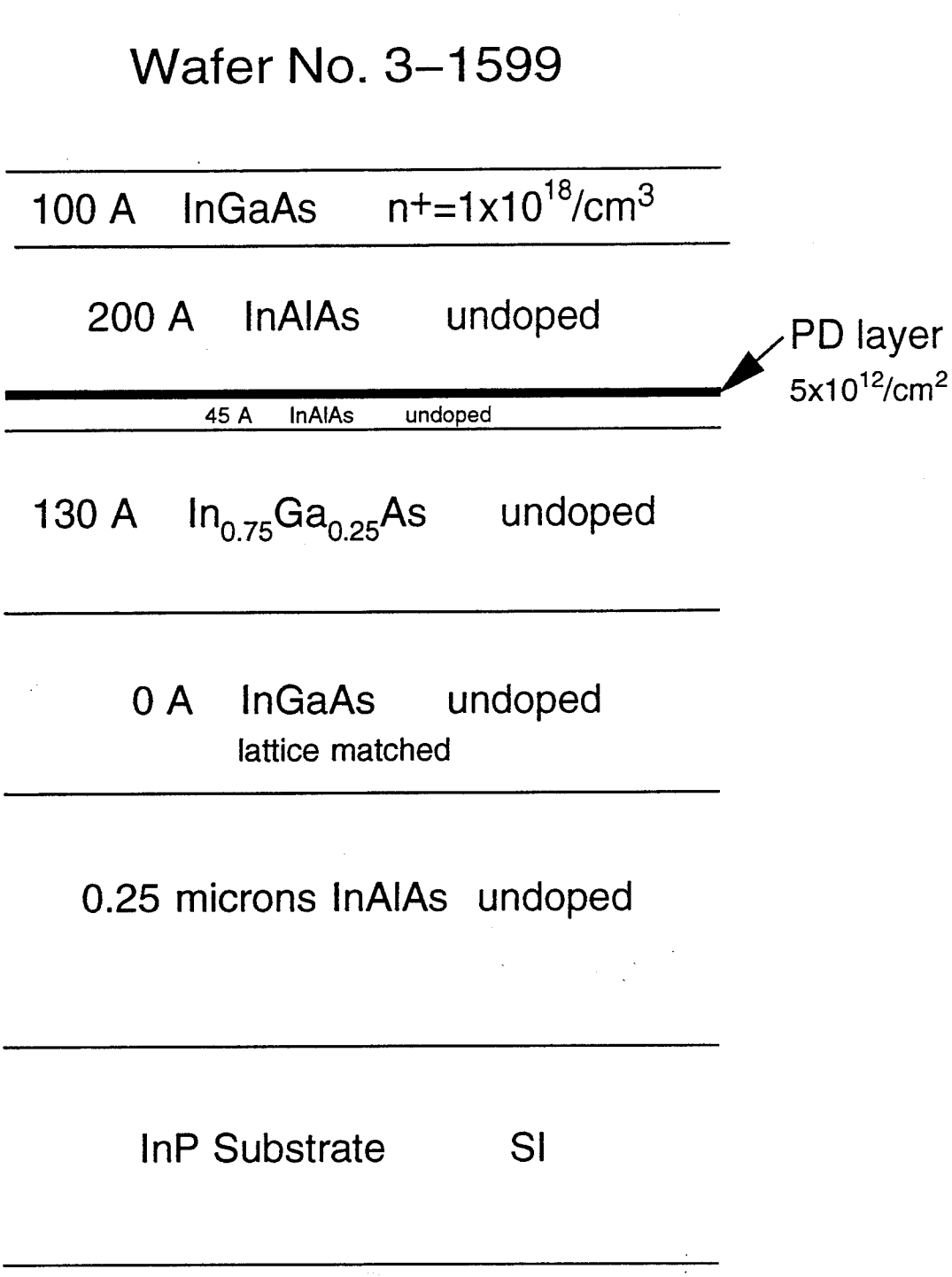


Figure 45. Structure for wafer no. 3-1599.

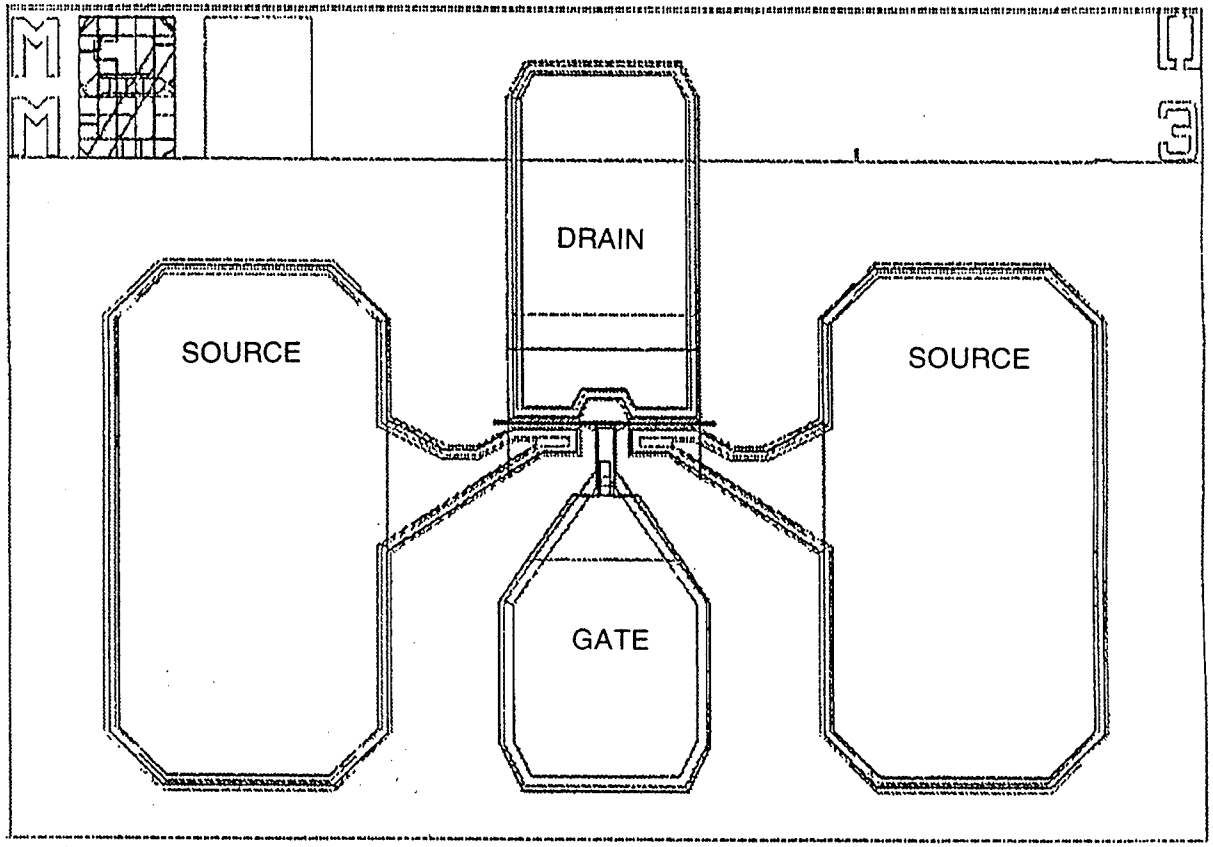


Figure 46. Device layout for InP HEMT with T-gate.

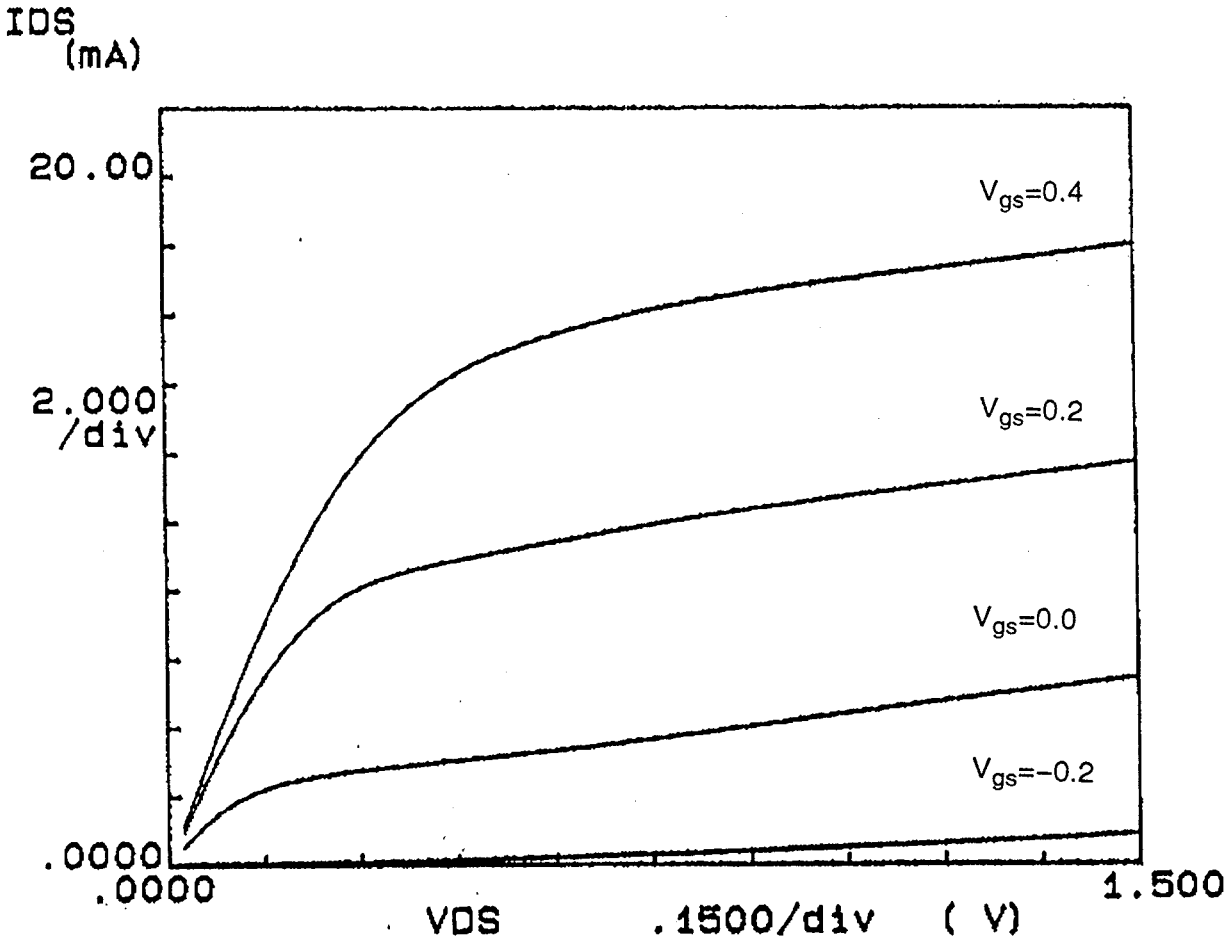


Figure 47. Measured current-voltage characteristics for device no. 3-1603.

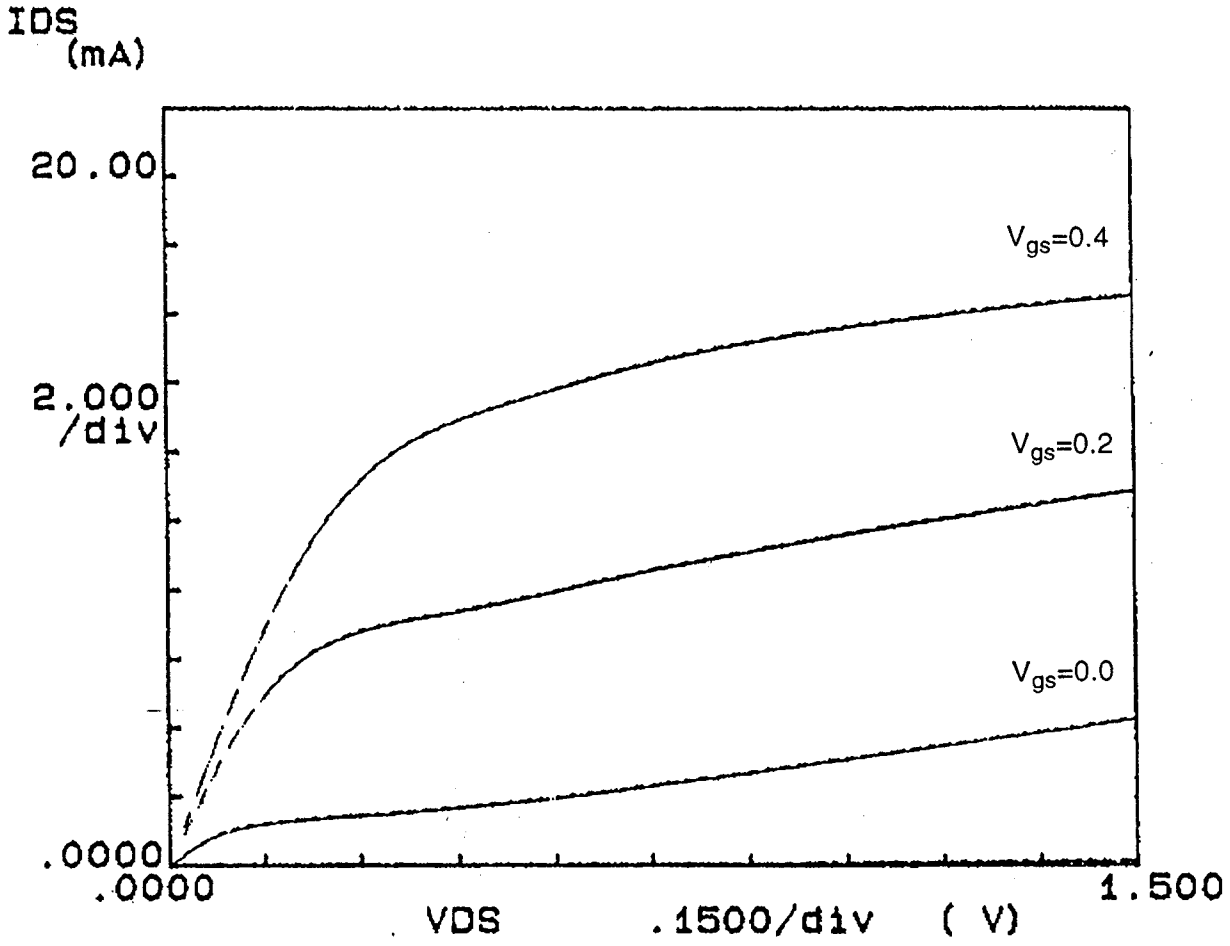


Figure 48. Measured current-voltage characteristics for device no. 3-1605.

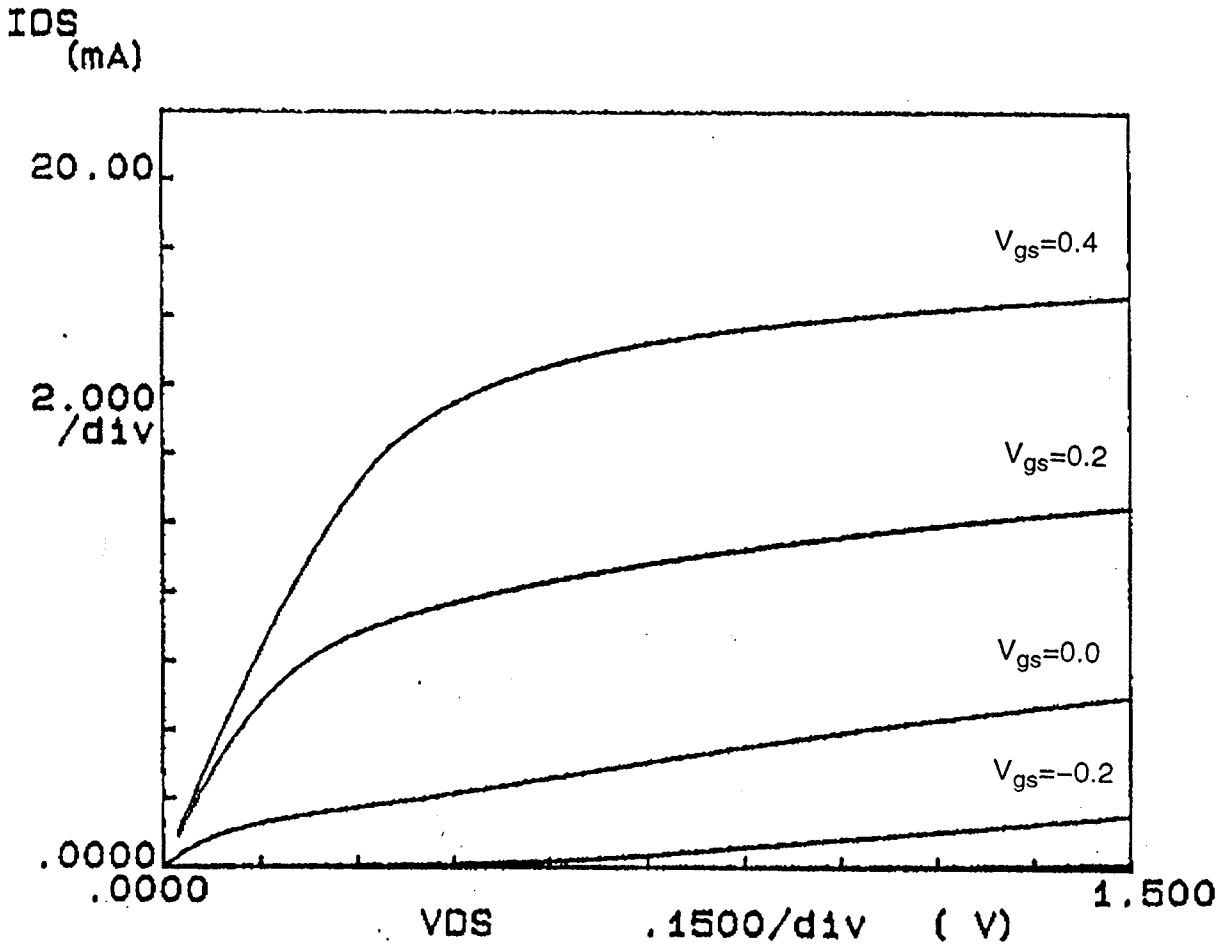


Figure 49. Measured current-voltage characteristics for device no. 3-1800.

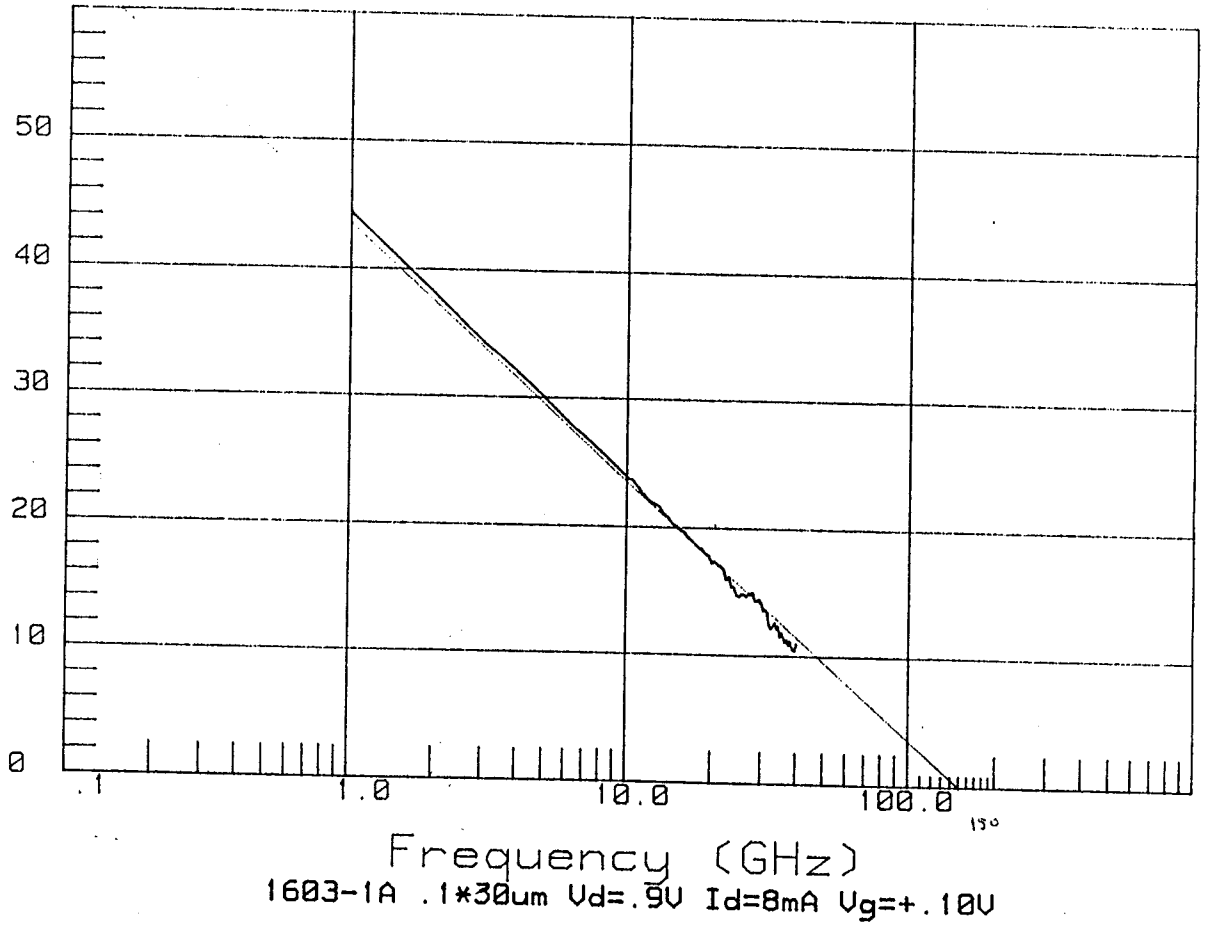


Figure 50. Gain vs. frequency for device no. 3-1603.

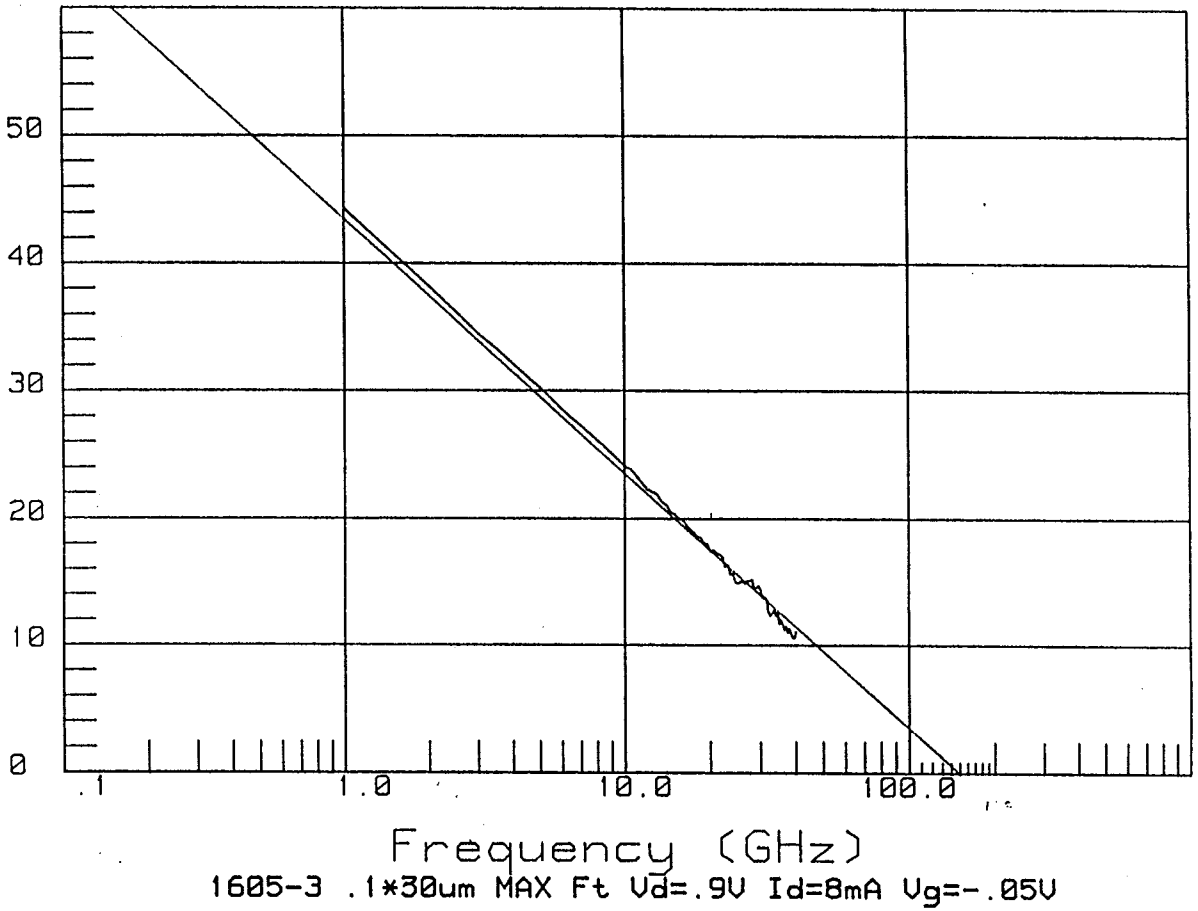


Figure 51. Gain vs. frequency for device no. 3-1605.

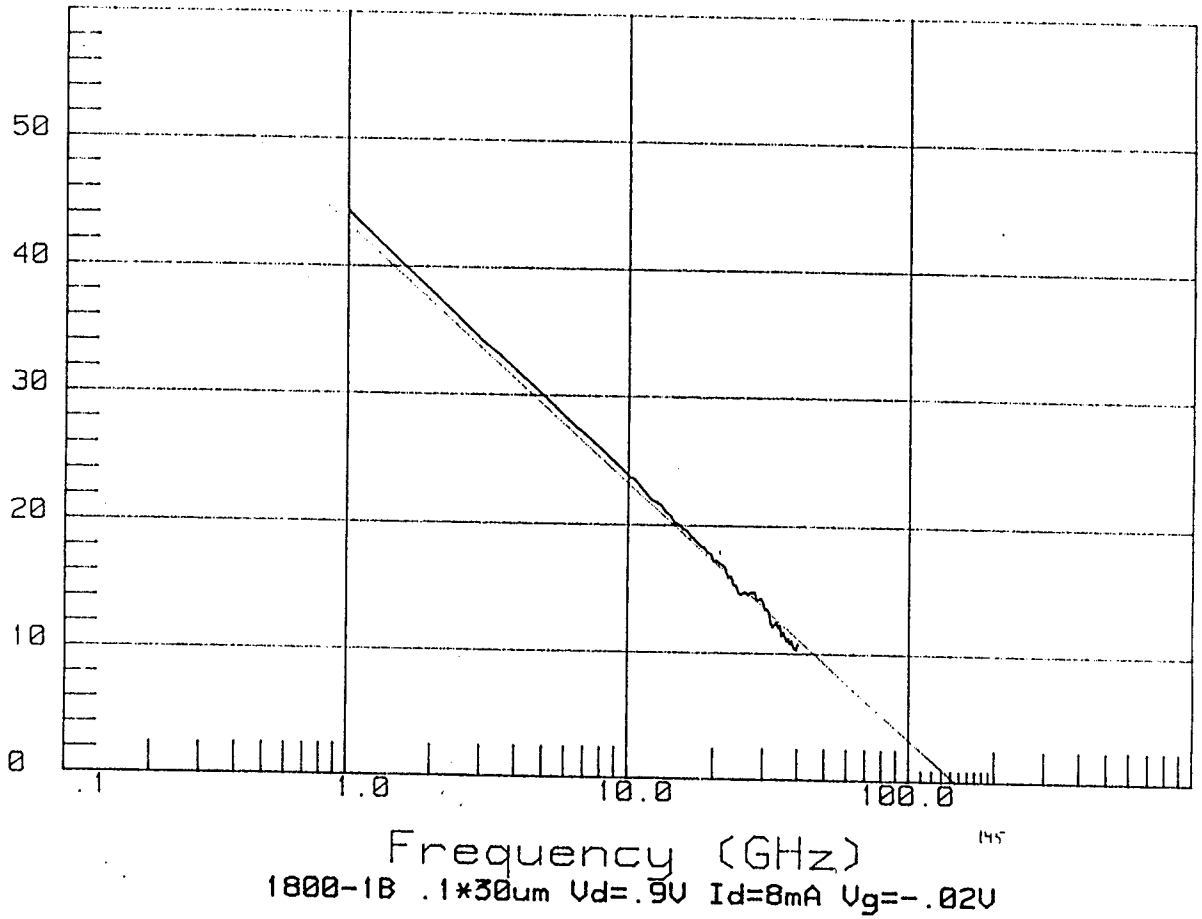


Figure 52. Gain vs. frequency for device no. 3-1800.

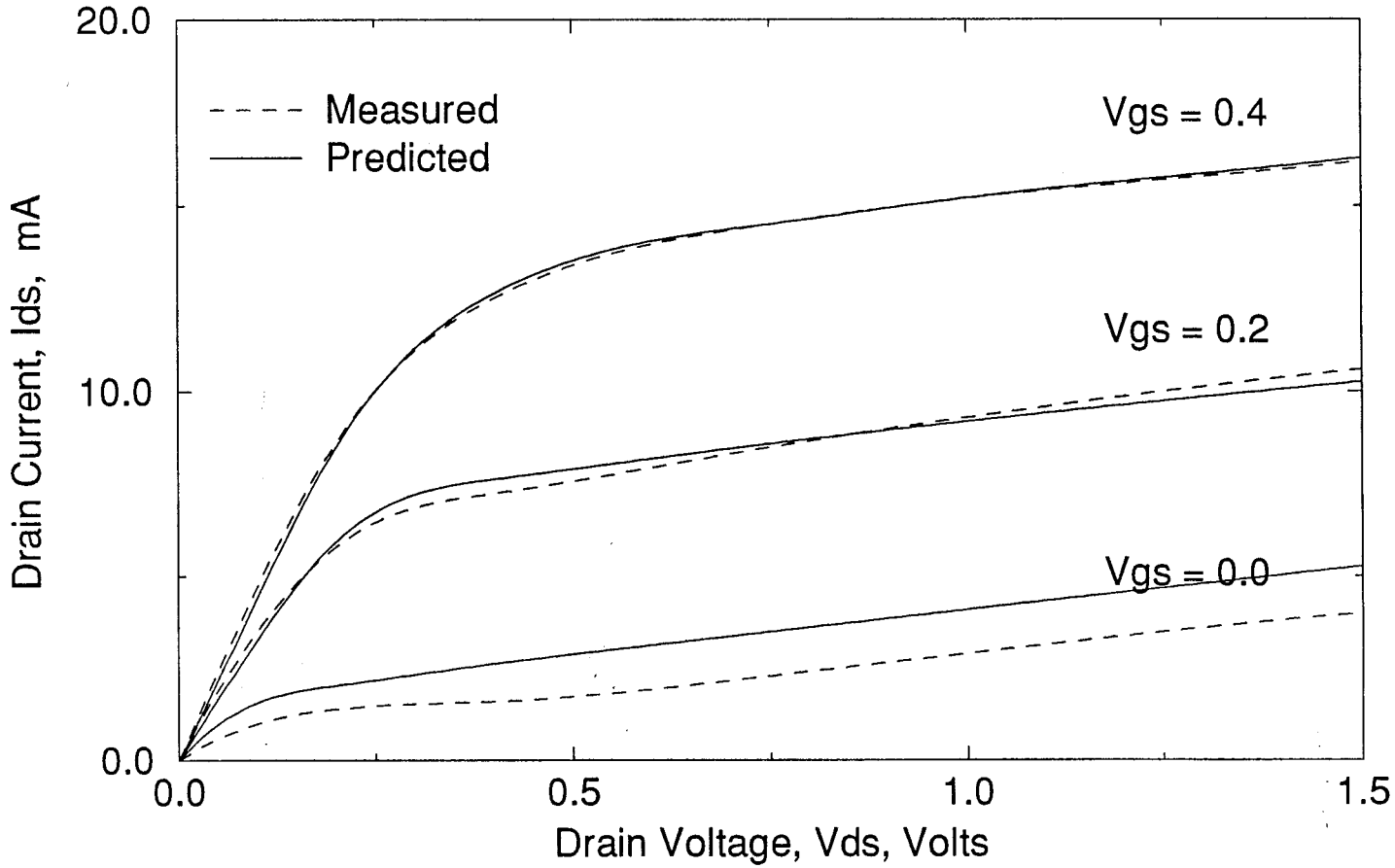
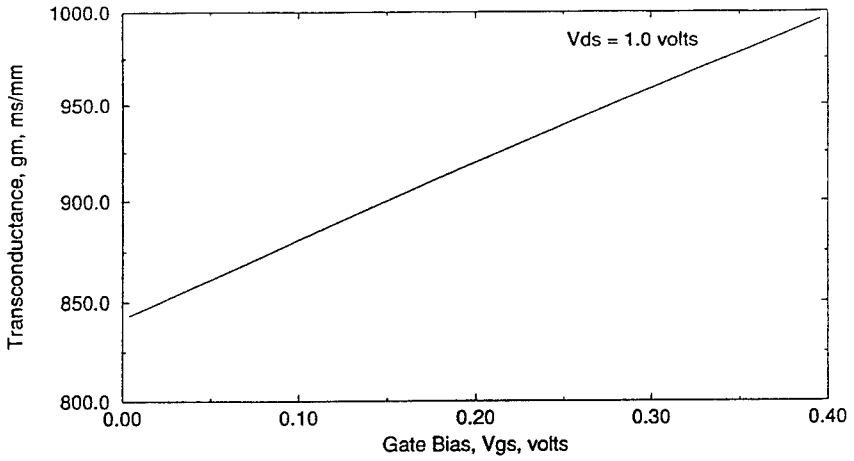
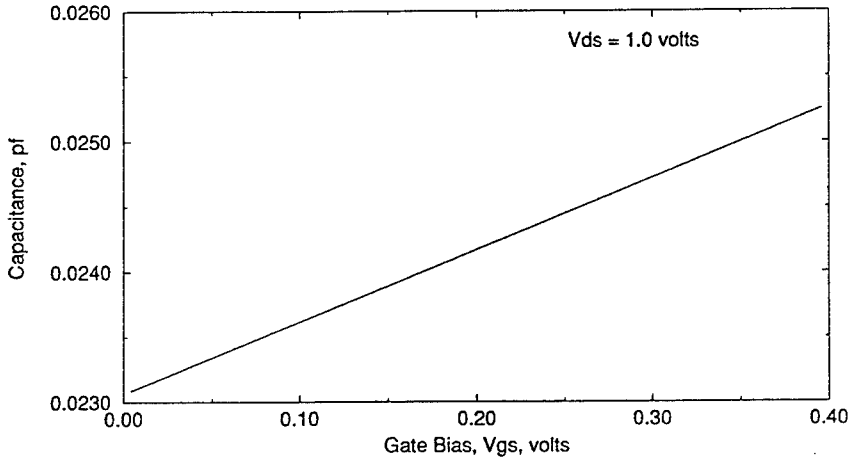


Figure 53. Comparison between measured and predicted characteristics for device no. 3-1605.





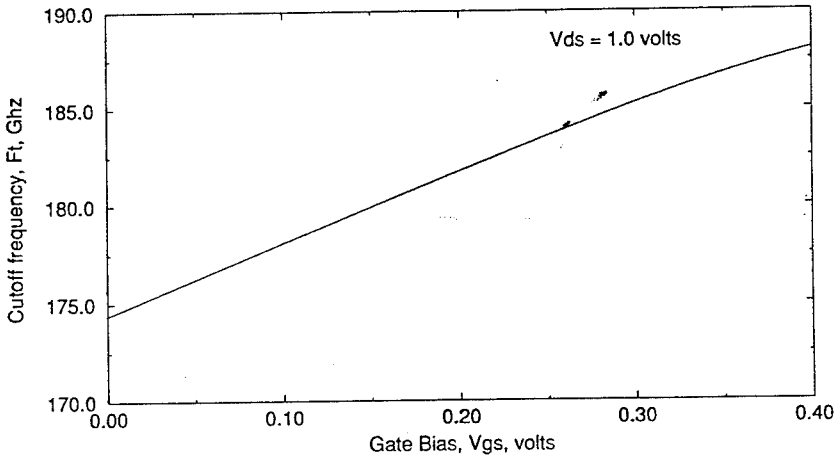


Figure 54. Predicted transconductance, capacitance and cut-off frequency for device no. 3-1605.

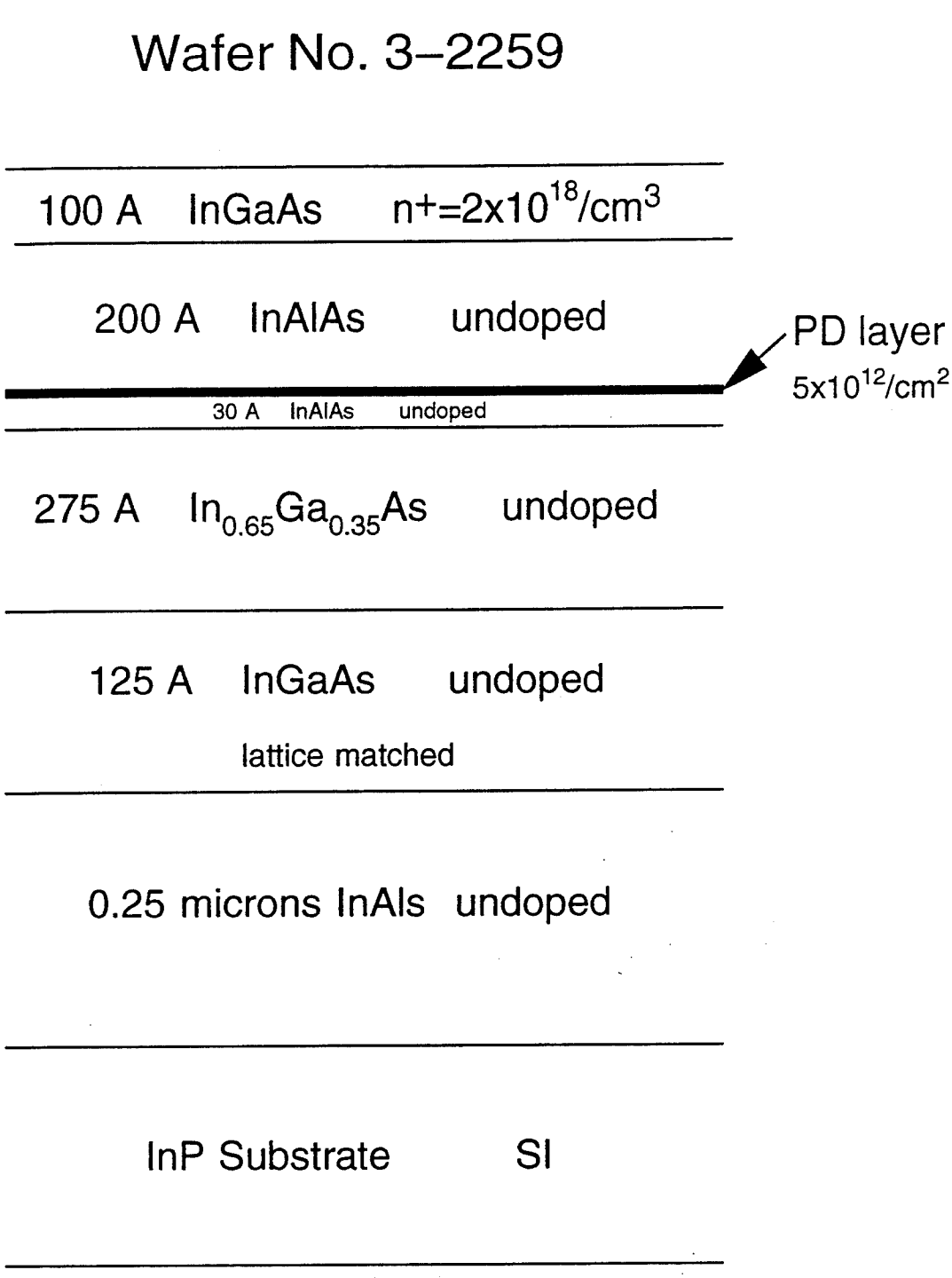


Figure 55. Structure of optimized HEMT wafer.

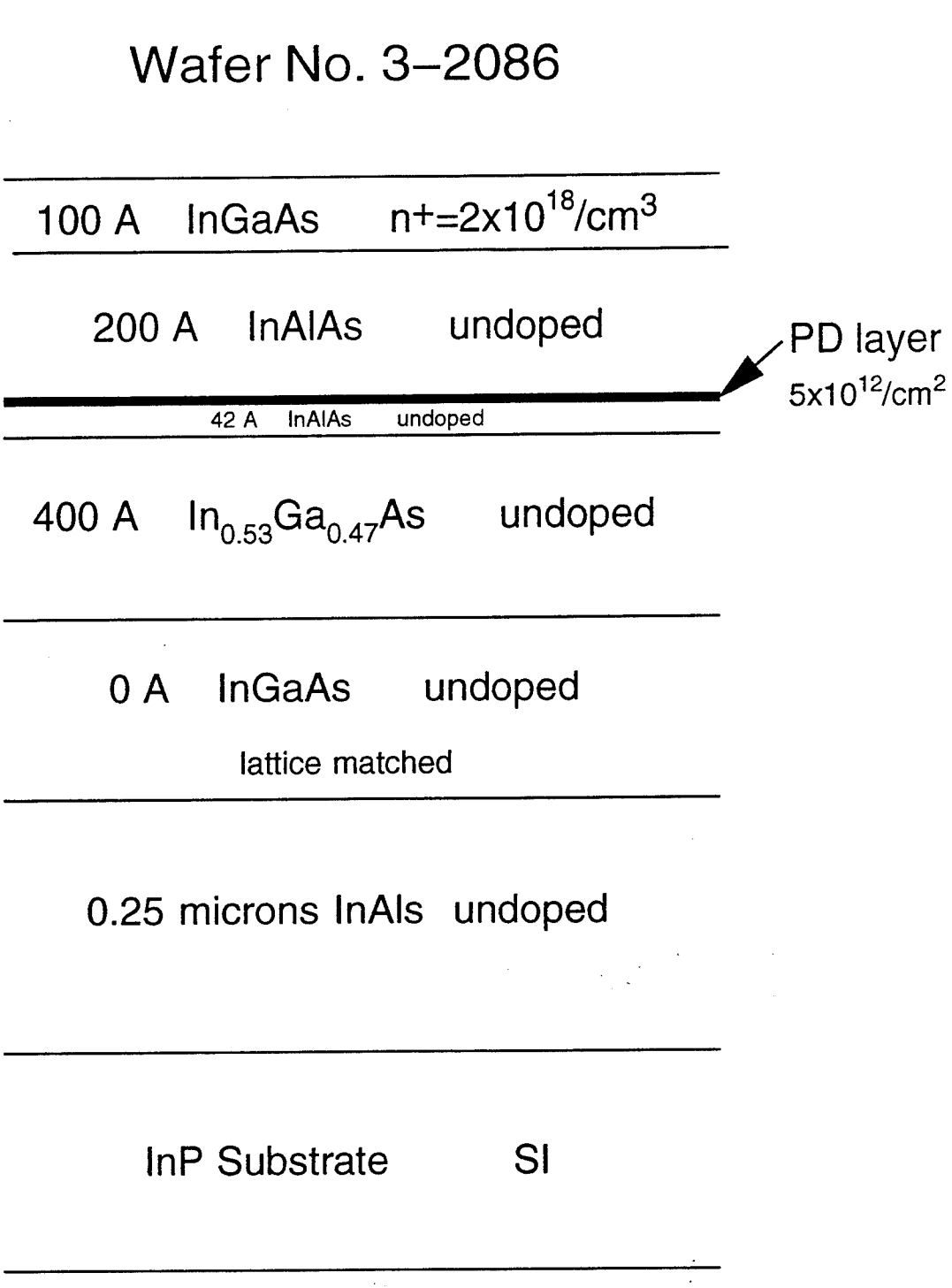


Figure 56. Structure of control HEMT wafer.

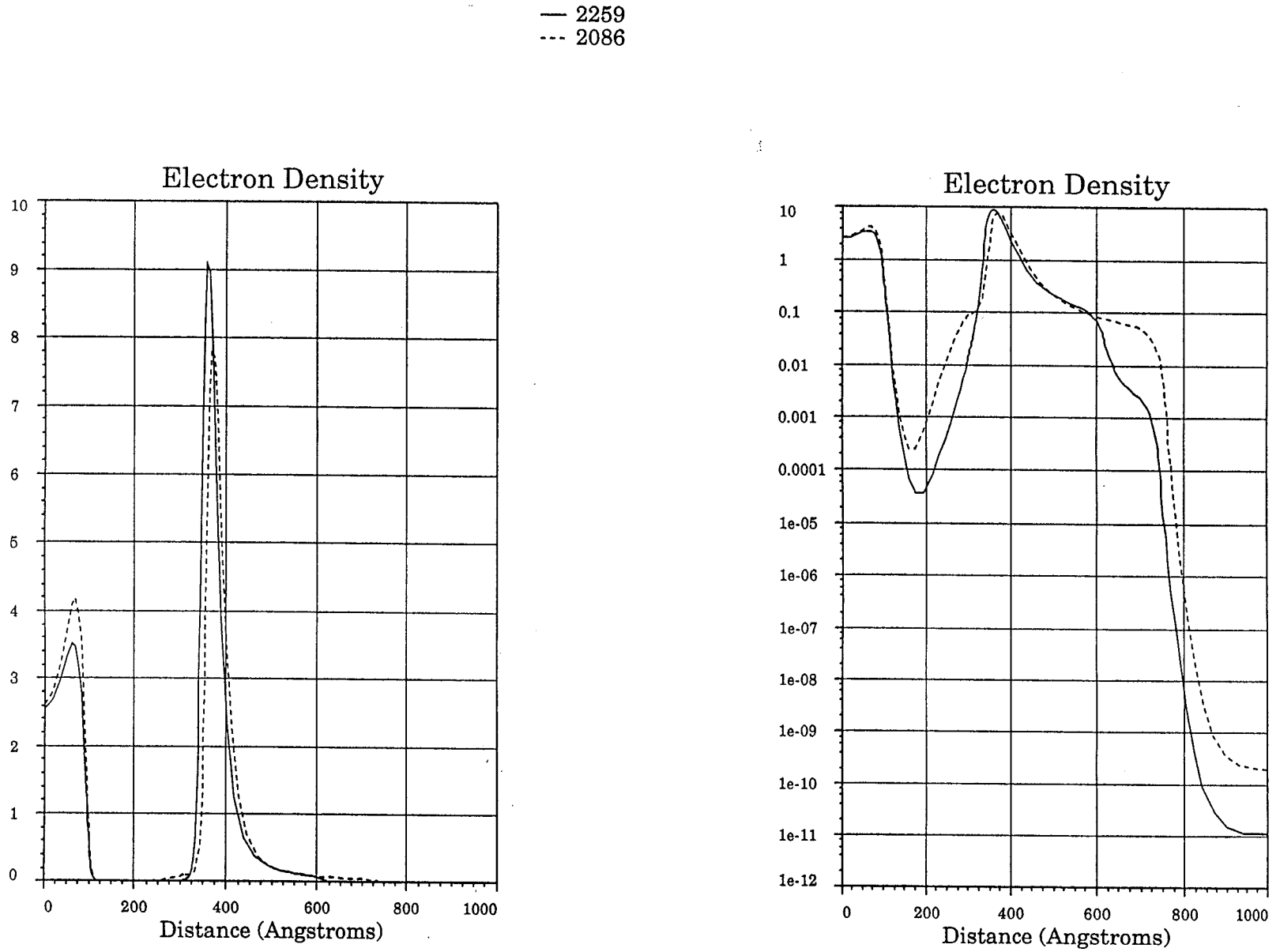


Figure 57. Comparison between predicted density distribution in optimized and control wafers.

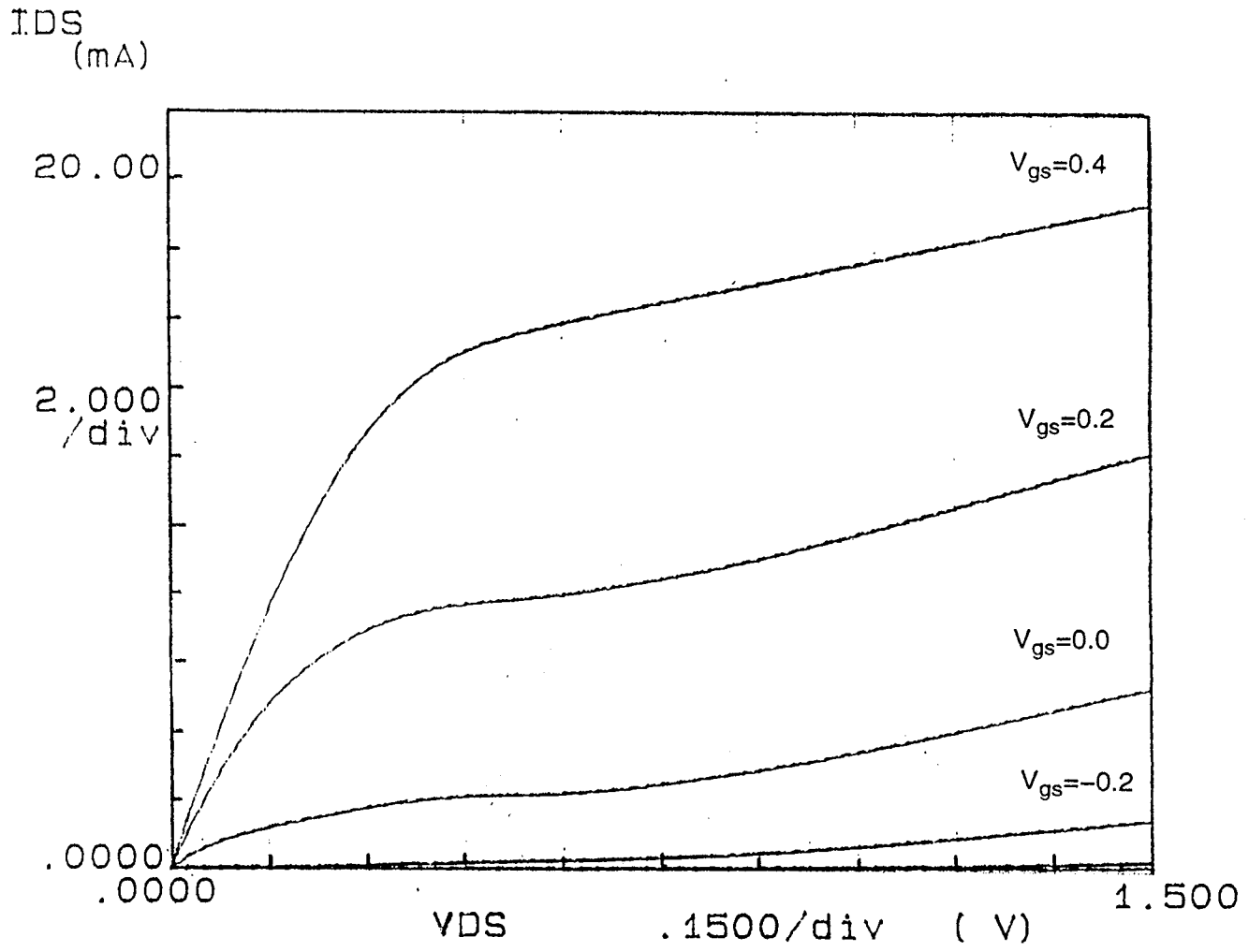


Figure 58. Measured current-voltage characteristics of optimized HEMT.

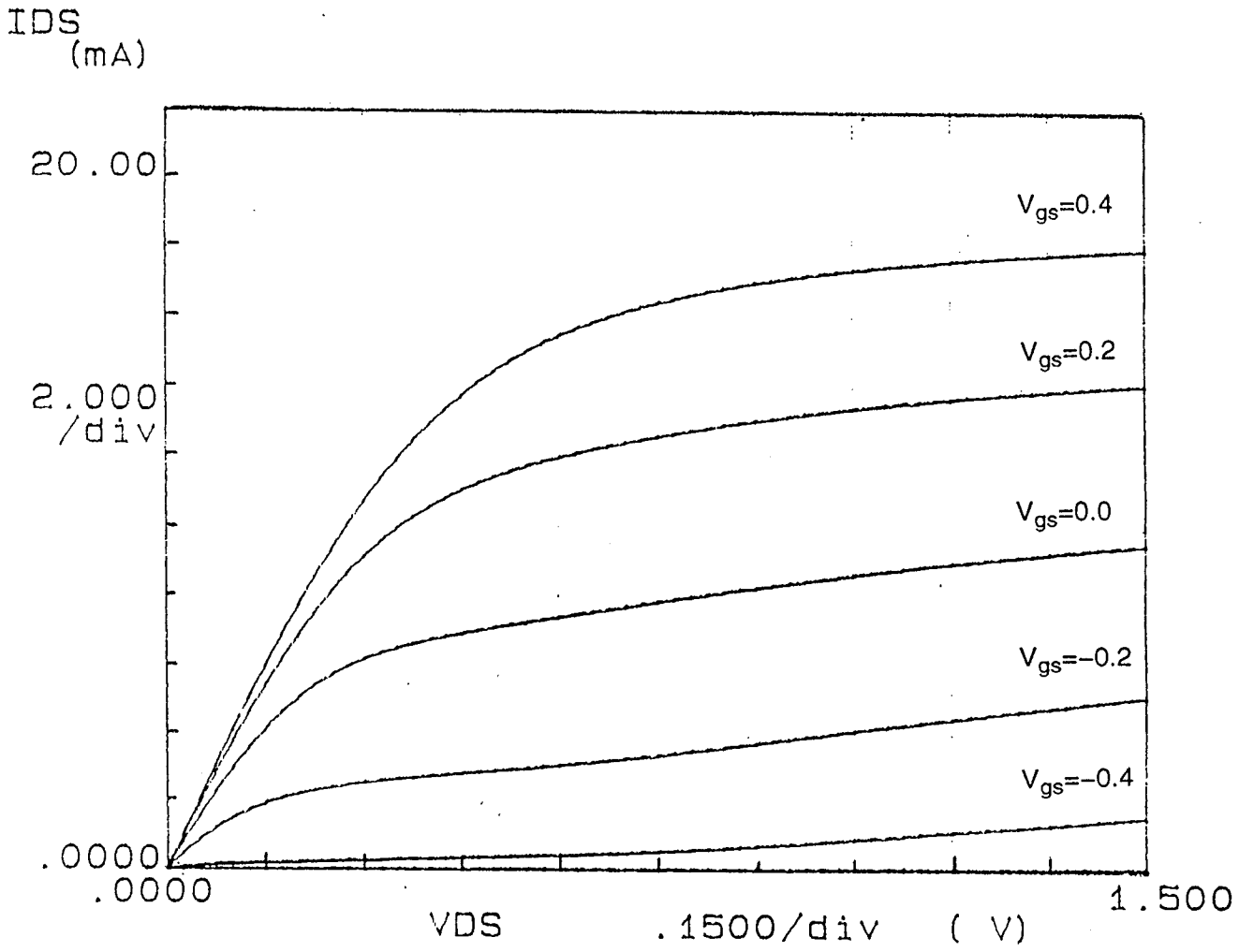


Figure 59. Measured current-voltage characteristics of control HEMT.